

Applications of micron-scale passive diamond layers for the integrated circuits and microelectromechanical systems industries¹

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Abstract

The deposition of passive diamond layers of thickness comparable to 1 μm directly within integrated electronic and optoelectronic circuits and microelectromechanical systems promises to improve their figures of merit, in particular those influenced by heat conduction. This application of diamond poses major challenges for deposition research, yet offers important thermal design advantages over the more common application of thick diamond plates in electronic packages. This manuscript reviews research on using micron-scale passive diamond layers in microfabricated circuits and sensors and predicts the impact of these layers on temperature fields and figures of merit. The predictions benefit from a review of thermal conductivity and boundary resistance studies for micron-scale diamond layers, with a focus on those fabricated using temperatures and nucleation methods that promise compatibility with VLSI technology. © 1998 Elsevier Science S.A.

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1. Introduction

When considering the potential impact of chemical vapor deposited (CVD) diamond layers on the performance and reliability of electronic systems, it is helpful to separate the applications into three groups based on the challenges they pose for deposition technology and the promise they offer for thermal design [1]. Table 1 shows that thick, passive diamond plates are improving thermal conduction in the packaging of high-power semiconductor laser arrays and high-frequency amplifiers. A second class of passive applications uses much thinner diamond layers deposited within micrometers of active Si and GaAs regions in microfabricated circuits, sensors and actuators. These applications have received relatively little attention because of the difficulty of fabricating high-quality diamond using temperatures and nucleation methods compatible with conventional integrated circuit (IC) technology. This concern is augmented by the traditionally conservative approach taken by the semiconductor industry with respect to the processing of commercial ICs and microelectromechanical

systems. Within the past 5 years, however, the industry has recognized that future improvements in performance and reliability may only be possible through the use of new materials. This is resulting in a unprecedented quantity of applied research at semiconductor firms and their suppliers on the integration of polymers, porous oxides and novel metallization into ICs and MEMS. Over the same period, research on the deposition of micron-scale diamond layers has been improving step coverage, increasing growth rates and reducing deposition temperatures. The progress in diamond deposition research and the changing research focus in the semiconductor industry indicate that the second class of applications discussed in Table 1 warrant closer attention.

The deposition of micron-scale passive diamond layers directly within integrated electronic and optoelectronic circuits and microfabricated sensors and actuators offers substantial thermal design advantages over the more conventional application of relatively thick diamond plates in electronic packages. A major benefit is the fact that diamond can be deposited within fractions of a micrometer of active regions, where heat is generated. This increases the relative impact of diamond on the temperature fields within and near active regions, particularly during rapid transient heating. As a result, diamond thin films in MEMS can strongly reduce thermal

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Table 1
Applications of CVD diamond layers in electronic systems

	First generation: passive plates	Second generation: passive films	Third generation: active layers
Layer thickness	100–500 μm	0.1–10 μm	0.1–500 μm
Example applications	Mount for high-power devices, chip carrier for logic circuitry	Buried insulator in SOI circuit, supporting layers for bolometers	Microwave transistor, thermistor
Competing materials	Aluminum oxide, aluminum nitride, copper	Silicon dioxide, silicon nitride, aluminum nitride	Silicon, gallium arsenide, silicon carbide, gallium nitride
Impact on thermal conduction	Improvement in macroscopic packaging	Improvement within micrometers of active regions	Improvement within active regions
State of development	Many applications in or nearing production	Applied research	Basic research (transistors) Applied research (sensors)

time constants while making possible the higher operating temperatures associated with the large bandgap and the chemical stability of the material. These benefits for MEMS technology are particularly interesting for micro-fabricated thermistors and low-temperature bolometers. Another consideration is that in contrast to diamond plates, which compete with plates made using a variety of high thermal conductivity materials including single-crystal aluminum nitride and copper, passive diamond thin films compete with amorphous and nanocrystalline oxide and nitride films which have thermal conductivities that are orders of magnitude smaller than those readily achieved in micron-scale diamond layers. This large contrast allows the peak temperature rise in semiconductor circuits to be strongly reduced by replacing oxide passivation with diamond. This reduction in the temperature is particularly interesting for circuits that must withstand transient heating, such as high-power logic and analog devices, and circuitry that must withstand electrical overstress phenomena (EOS).

The integration of diamond layers on or within many of the microdevices described in Table 1 poses major processing challenges in the areas of nucleation, growth temperature, growth rate and etching. The use of diamond as passivation of Si or GaAs devices requires growth of high-quality material at temperatures well below 400 °C, although the optimal temperatures for diamond CVD usually exceed 800 °C. This review will discuss recent progress on the deposition of diamond with reasonably high thermal conductivity using temperatures near 500 °C, although at these temperatures the growth rate is considerably below 1 $\mu\text{m h}^{-1}$. Also challenging is the problem of achieving uniform diamond nucleation on substrates with nonflat surfaces consisting of several materials, which is necessary for diamond passivation. Promising examples of diamond step coverage and nucleation have been achieved using mechanical pre-treatment, yielding the layers depicted in Fig. 1.



Fig. 1. Cross-sectional electron micrograph of a polysilicon bridge passivated using CVD diamond. The diamond was nucleated using exposure to a diamond-particle slurry and ultrasound, and was grown near 400 °C (courtesy of H. Güttler et al., Daimler-Benz AG).

Because the properties of micron-scale diamond layers depend very strongly on the processing details, it has been difficult to quantitatively assess the potential impact of these layers on temperature fields in specific microdevices. The thermal analysis of microdevices containing micron-scale passive diamond regions is complicated by the large densities of grain boundaries and stoichiometric and phase impurities. These yield thermal conductivities that are not well predicted by models developed for relatively thick diamond plates and are strongly anisotropic and nonhomogeneous. Thermal analysis must also consider the impact of thermal boundary resistance, for which there are very few data available, and of phonon scattering on layer boundaries, which can be very important at low temperatures.

This manuscript aims to provide an overview of the potential benefit of the second generation applications in Table 1. In support of this goal, Section 2 reviews thermal conductivity, diffusivity and boundary resistance studies for diamond layers of thickness between

0.2 and 10 μm with a focus on data and predictions of direct relevance to IC and MEMS applications. Models and data relating diamond thermal properties to the grain structure in the near-interfacial region provide insight into the highly anisotropic, nonhomogeneous thermal conductivity and the effective boundary resistance resulting from near-interfacial disorder. The isotropy and homogeneity are shown to be particularly sensitive to the deposition details and to the substrate material. Section 3 describes the fabrication technology available for composite silicon–diamond substrates, diamond passivation and diamond/silicon sensors and actuators and quantitatively predicts the impact of the diamond on temperature fields in these devices. The calculations are based on the models developed in Section 2 and consider the layers fabricated using temperatures and nucleation methods compatible with the microdevice being considered.

2. Thermal transport properties of micron-scale diamond layers and their boundaries

The thermal transport properties of diamond layers thinner than 10 μm deposited on non-diamond substrates are strongly anisotropic, often nonhomogeneous, and in general considerably inferior to those of gem-quality diamond crystals. This results from the relatively high concentrations of imperfections in these layers, particularly within tens of nanometers of the layer-substrate interface, from the density, orientation and integrity of grain boundaries, and from the importance of phonon scattering on layer boundaries. There have been previous reviews of the thermal transport properties of diamond layers by Graebner [2] and by Plamann and Fournier [3]. Those reviews provide much information about the impact of diamond growth conditions on heat transport by focussing on free-standing layers thicker than a few micrometers. However, the data and modeling featured in those previous reviews are not sufficient for understanding heat transport in composite semiconductor devices and sensors containing passive diamond, which are featured in the present manuscript. These composite structures can contain diamond layers thinner than 1 μm and have temperature fields strongly influenced by conduction normal to diamond boundaries with other materials, which cannot be interrogated using free-standing samples. To remedy this situation, this section supplements the past reviews by focussing on the transport properties of layers thinner than 10 μm . The problem of thermal resistance at diamond-substrate boundaries and the large impact that the nucleation method exerts on this property is specifically addressed. The experimental methods described here have been reviewed previously [2–6].

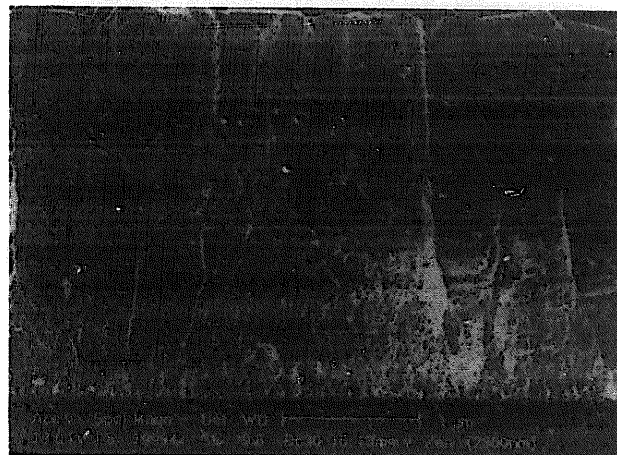


Fig. 2. Cross-sectional electron micrograph of a diamond layer deposited at 800 °C and nucleated using a bias voltage.

2.1. Impact of nucleation method and microstructure on conductivity

The key to understanding heat conduction in thin diamond layers lies in the grain structure, which can be observed in electron micrographs such as that shown in Fig. 2. The grain structure describes the orientation and density of grain boundaries, near and in which point defects and regions of phase impurity collect during the deposition process [7]. The grain structure is approximately depicted in Fig. 3, which shows that the lateral grain dimensions increase with increasing separation from the substrate. This increase can be described using the characteristic lateral grain dimension, $d_G(z)$, which is the average separation between intersections of a reference line parallel to the substrate at height z with grain boundaries. The grain dimension at the layer-substrate interface, d_{G0} , is inversely proportional to the square root of the grain nucleation density and depends strongly on the details of the nucleation process. High densities are common for layers nucleated using a bias voltage between the process gases and the substrate. In these layers, the grain structure at the layer-substrate interface can be very complex because of the high initial concentration of diamond nuclei competing for growth

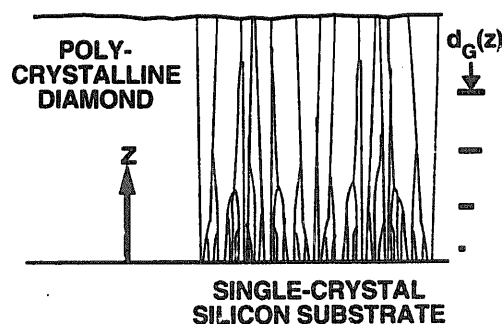


Fig. 3. Approximate schematic of the grain structure in a micron-scale diamond layer deposited on silicon.

space. Alternative nucleation methods are based on mechanical pretreatment, such as exposure to acoustic excitation in the presence of a diamond-particle slurry.

The nonhomogeneity of the thermal conductivity in the direction normal to the substrate is determined by the spatial variation of the grain size and the dominant grain-boundary orientation. Within the first few hundreds of nanometers above the diamond–substrate interface, grains compete and terminate as they grow and as a result are relatively small and have boundaries oriented randomly with respect to the substrate. A simple and effective approach for modeling the rate of grain growth uses a linear approximation

$$d_G = d_{G0} + \gamma z \quad (1)$$

with values of γ estimated from electron micrographs. Although more complicated forms of the grain size variation can be introduced, Eq. (1) is adequate for illustrating the dependence of heat transport properties on the microstructure of the thin layers under study. More detailed modeling [8] accounts for the thickness at which the onset of predominantly-columnar grains occurs and the thickness of disordered material near the substrate.

The anisotropy of the thermal conductivity of diamond plates thicker than ca 10 μm has been well documented [2] and is a result of the columnar grain structure. Heat conducts much more effectively along the grains, normal to the substrate, than it conducts normal to the grain boundaries in the plane of the substrate. The situation is rather more complicated in diamond films of thickness less than 10 μm , in which the anisotropy is a complex function of the spatial variation of the grain size, the fraction of the layer in which grains are predominantly columnar, and the magnitude of the boundary resistances at the top and bottom surfaces of the layer. The impact of the columnar grain structure can be overshadowed by thermal boundary resistances and a large variation of the grain size with the coordinate z , both of which tend to make the effective conductivity along layers larger than the effective conductivity normal to layers. This can be understood by considering the effective thermal conductivities for transport in the directions normal to and along a thin layer, k_n and k_a , respectively. In a thin film whose conductivity varies with the coordinate z , k_a is the spatial average of the local conductivity within the layer. The effective conductivity k_n is the inverse of the spatial average of the *inverse* of the out-of-plane conductivity in the layer, which must always be less than k_a in an isotropic medium. Boundary resistances further reduce the effective conductivity k_n compared to k_a , which is not influenced by conduction normal to boundaries. However, the columnar grain structure causes the conductivity to be anisotropic within the layer and larger in the normal direction. It is important to distinguish

columnar grains from those near the substrate–layer interface with randomly-oriented boundaries, which do not contribute to local anisotropy. The existing data suggest that the two competing effects, that is, nonhomogeneity and columnar orientation, yield an anisotropy ratio whose magnitude can vary by orders of magnitude and depends strongly on the deposition details. At present we are aware of only one set of layers of thickness below 5 μm whose conductivities have been measured in both directions. These data will be discussed in Section 2.3 and show conductivity ratios $k_a/k_n < 0.1$.

2.2. Measurements of the normal thermal conductivity and diffusivity and the boundary resistance of layers thinner than 10 μm

Two independent methods measure the vertical thermal conductivities of metallized diamond films on silicon. The *Joule-heating method* [9] monitors the temperature rise for ca 300 μs during a electrical heating pulse in a patterned metal microbridge deposited on the diamond–silicon composite. The microbridge temperature is calculated from its measured transient electrical resistance. The *laser-heating method* [9,10], depicted in Fig. 4, uses laser-reflectance thermometry to monitor the transient temperature rise at the surface of the metal for ca 1 μs after a laser-heating pulse of duration near 10 ns. In both electrical and laser-heating methods, the thermal resistance for conduction normal to the diamond layer, R_T , is extracted from the measured response by analyzing transient thermal conduction in the multi-layer system. The laser-heating technique was applied extensively by Verhoeven et al. [11,12] to study thermal properties of thin diamond films as a function of deposition temperature and nucleation method. The layers deposited at temperatures near 500 $^\circ\text{C}$ were nucleated mechanically and exhibited columnar grain orientation. The layers deposited at 800 $^\circ\text{C}$ were nucleated using a bias voltage, were highly-oriented, and had dominant

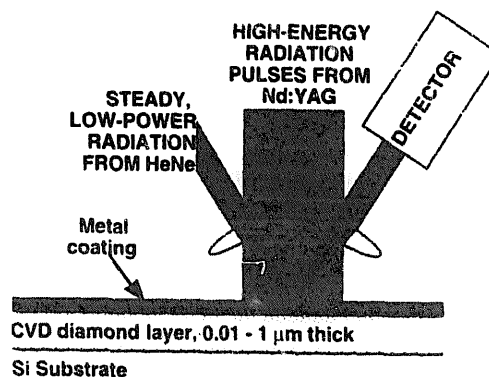


Fig. 4. Schematic of an experimental method for measuring the vertical thermal resistance of diamond layers.

$\langle 100 \rangle$ crystal structure like the silicon substrate. This work demonstrated that the short timescale of laser heating allows both the diffusivity and the boundary resistance to be extracted from the shape of the decaying surface temperature. The largest measured diffusivities were observed in the high-temperature-deposited layers of 4 μm thickness and correspond to a conductivity of $600 \text{ W m}^{-1} \text{ K}^{-1}$. The films deposited near 500°C had diffusivities corresponding to conductivities close to $100 \text{ W m}^{-1} \text{ K}^{-1}$.

2.3. *Measurements of the thermal conductivity and diffusivity along layers thinner than 10 μm*

There have been several studies of the in-plane thermal conductivities near room temperature for films of thickness $< 10 \mu\text{m}$. Herb et al. [13] determined the thermal conductivities from the minimum temperature measured in free-standing diamond bars of thickness near $2 \mu\text{m}$ that were suspended between two heated posts. This method yielded the conductivity at temperatures near 373 K. These authors found that the thermal conductivity varied between 300 and $1130 \text{ W m}^{-1} \text{ K}^{-1}$ and increased rapidly with decreasing values of the methane concentration percentage used during deposition, which varied between 0.05 and 0.5%. Graebner et al. [14] reported room-temperature thermal-conductivity data for films of thicknesses between ca 3 and $13 \mu\text{m}$. The measurements were performed by etching the silicon substrate from beneath a rectangular section of the diamond, onto which a bridge was deposited and patterned to provide heat generation. The thermal conductivity of the free-standing diamond film was deduced from the temperature distribution resulting from heating in the bridge. The temperature distribution was measured using patterned thermocouple bridges. The layers were processed using methane concentration between 0.5 and 4% and had thermal conductivities that varied between ca 190 and $600 \text{ W m}^{-1} \text{ K}^{-1}$. Graebner [2] showed that the conductivity data from these two studies are consistent when plotted as a function of the methane-to-hydrogen concentration ratio used during deposition.

Käding et al. [15] measured the thermal diffusivities of films of thicknesses near $5 \mu\text{m}$ using the transient thermal grating technique with a very small spatial period of the heating intensity. This technique induces a harmonic spatial variation of rate of flash heat deposition at the sample surface using the interference of radiation from a Nd:YAG laser incident from separated paths. The temporal decay of the spatial variation in the temperature field is detected through the relaxation of the surface displacement using the deflection of an independent probe laser. The temporal decay is governed predominantly by the lateral thermal diffusivity of the sample within a depth comparable with the spatial period of heat generation, which can be varied by

altering the angle between the paths of the interfering beams. Käding et al. [15] extracted the diffusivity of both the diamond film and the underlying substrate by varying the depth of interrogation, which is governed by the spatial period of the laser-induced heat generation. The thermal conductivities calculated from the diffusivities in this study and the specific heat, which can be approximated as that of bulk diamond [16], are slightly less than that of silicon, $150 \text{ W m}^{-1} \text{ K}^{-1}$. Verhoeven et al. [12] used the transient thermal grating technique to measure the lateral diffusivities of highly-oriented films and used the data to indicate a large diffusivity anisotropy, with the value of the in-plane property being an order of magnitude smaller.

Plamann et al. [17] used the mirage technique to measure in-plane diffusivities for free-standing layers of thickness between 0.3 and $6 \mu\text{m}$ that were deposited using varying methane-to-hydrogen concentration ratios. They used a laser beam to induce periodic heating at the sample surface with a frequency near 20 Hz. A laser beam traveling parallel to the layer surface was deflected due to changes in the refractive index of the gas near the surface induced by heating from the sample. The sample diffusivity was calculated from the phase and amplitude of the deflection, which varies with the separation between the two laser beams. The same technique was applied by Bachmann et al. [18] to study effects of varying plasma chemistry during the deposition and it was observed that the presence of gases other than hydrogen adversely affects thermal properties of the resulting films.

2.4. *Modeling*

Heat transport in dielectrics can be modeled using phonon transport theory, which accounts for energy transport by atomic vibrational waves. The transport theory yields an expression for the thermal conductivity, for which the reader is referred to previous work [2,19], which is governed by the rate of phonon scattering. A major challenge for modeling heat transport in polycrystalline diamond layers is to appropriately account for the impact of the grain size and orientation on the rate of phonon scattering. The correct approach is not simply a geometrical problem involving phonon scattering on the boundaries of grains with varying size and shape. Temperature-dependent thermal conductivity data indicate that scattering on grain boundaries is not a dominant effect [20]. The explanation is suggested by electron micrographs of single diamond grains [7], which indicate that large concentrations of imperfections can collect within hundreds of nanometers of grain boundaries. This can be quantified using the following expression for the phonon scattering rate

$$[\tau(z, T)]^{-1} = [\tau_U(z, T)]^{-1} + [\tau_{\text{HD}}(z)]^{-1} + [\tau_{\text{GB}}(z)]^{-1} \quad (2)$$

Terms in Eq. (2) depend on the phonon angular frequency, the temperature, T , and the position in the layer, z . The first term on the right is due to phonon-phonon scattering. The second term on the right accounts for scattering on imperfections whose concentrations can be modeled as *laterally homogeneous*, that is, which are not present with greater concentration near grain boundaries. The second term is the sum of phonon scattering rates on defects of type j whose concentrations, c_j , are laterally homogeneous,

$$[\tau_{\text{HD}}(z)]^{-1} = v \sum_{j=1}^J \sigma_j c_j(z) \quad (3)$$

where v is the phonon velocity and σ_j is the scattering cross-section of the defect of type j . The cross-sections for scattering mechanisms are available from past work [2,21].

The third term on the right of Eq. (2) is the phonon scattering rate due to grain-boundaries, and can be interpreted using the dimensionless *grain-boundary scattering strength* [21],

$$\eta = \sum_{j=1}^J \sigma_j n_{\text{GB},j} \quad (4)$$

The number densities of imperfections of type j per unit grain-boundary area are denoted $n_{\text{GB},j}$ and have been estimated in past work from data for relatively thick layers [2].

Given Eqs. (2) and (3), the phonon scattering rates due to the grain boundaries can be determined from the characteristic grain dimension, d_G , and γ [21]. This calculation must take into account the grain boundary orientation. The scattering rate resulting from grains with randomly-oriented boundaries can be approximated by assuming that imperfections associated with a given grain boundary are distributed uniformly within grains. This yields the simplest expression for scattering rate, which is proportional to the grain-boundary scattering strength and inversely proportional to the grain dimension,

$$[\tau_{\text{GB}}(d, \omega)]^{-1} = \frac{2v_s \eta(d, \omega)}{d} \quad (5)$$

This simple approach is not appropriate for columnar grains, whose boundaries have a smaller effect on the thermal conductivity in the normal direction. This can be considered by collapsing all of the imperfections onto the grain boundaries, which yields

$$[\tau_{\text{GB}}(d, \omega)]^{-1} = \frac{2v_s}{\pi d} \left\{ 1 - \exp \left[-\frac{\pi^2}{4} \eta(d) \right] \right\} \quad (6)$$

Eq. (5) shows that for the assumption of a uniform distribution of imperfections within grains, the scattering rate can grow arbitrarily large with increasing values of the grain-boundary scattering strength. In contrast,

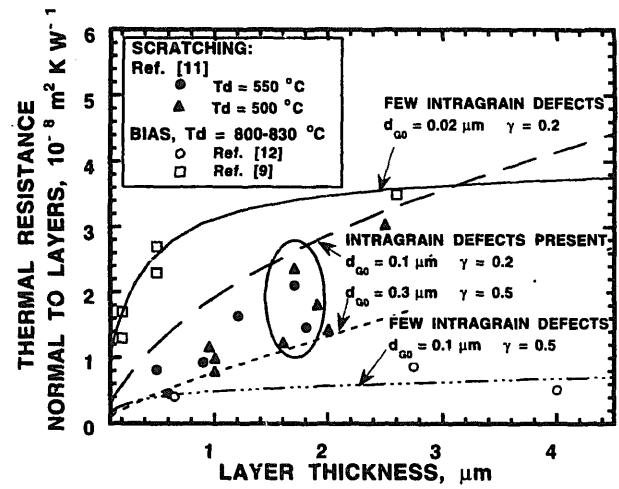


Fig. 5. Predictions and data for the thermal resistance for conduction normal to thin diamond layers on silicon.

Eq. (6) yields a scattering rate with an upper bound dictated by the grain size. Lower values of thermal conductivity are predicted if the scattering rate is calculated using Eq. (5) rather than Eq. (6). The concentration of grain boundaries per unit volume depends strongly on the grain size. While the grain boundary scattering strength may also vary, this model assumes that the grain size variation dominates the derivative of Eqs. (5) and (6) with respect to z . Eqs. (5) and (6) provide the necessary means for calculating anisotropic conduction properties in thin diamond layers.

2.5. Overview of conductivity data and comparison with modeling

Fig. 5 compares the data for the vertical thermal resistance of thin layers with the modeling described in Section 2.4. The vertical thermal resistance is the ratio of the layer thickness z_L to the effective observed thermal conductivity z_L/k_a , and is the sum of contributions due to the layer volume and its boundary. The model neglects scattering within grains, that is, the second term on the right in Eq. (2), compared to scattering on imperfections concentrated at grain boundaries. This approach appears to be best suited for the diamond layers deposited near 800 °C, which tend to consist of small diamond grains with low concentrations of internal imperfections. The agreement between the model and the data is reasonable for the layers deposited at high temperatures with vastly different values of the grain size and grain growth rate, which indicates that the simple modeling approach is warranted for layers grown under nearly optimal conditions. The layers deposited near 500 °C have thermal resistances that grow nearly linearly with increased thickness and therefore have thermal conductivities that vary slowly with thickness. However, agreement between the model and the data

for layers deposited near 500 °C can be achieved only through the use of an internal scattering term, that is, a finite value for the second term on the right in Eq. (2). This suggests that larger concentrations of imperfections are present within grains. Low deposition temperatures tend to inhibit the formation of diamond bonds and therefore introduce a larger concentration of non-diamond carbon in the deposited material [22,23]. From this modeling and data, it can be argued that the elevated level of intragrain defects in the layers deposited at low temperatures leads to the weak dependence of thermal conductivity on the grain size. For the layers shown in the Fig. 5 the predicted upper limit of thermal conductivity at room temperature is ca $200 \text{ W m}^{-1} \text{ K}^{-1}$, which is about an order of magnitude less than the bulk value. However, this value is more than two orders of magnitude higher than the thermal conductivities of common dielectric layers, such as silicon dioxide and silicon nitride.

Fig. 6 illustrates the usefulness of the modeling concepts developed in Section 2.3 for understanding lateral conduction along two sets of diamond layers deposited under different conditions. The calculations use Eq. (2) with the same grain-boundary scattering strength applied with reasonable success for conduction normal to layers deposited >800 °C in Fig. 4. The lateral thermal conductivity at low temperatures is influenced by phonon-boundary scattering and is calculated using a new solution to the phonon Boltzmann transport equation that accounts for a spatially-varying mean free path [21]. The only modeling parameter altered in Fig. 4 is the spatial rate of grain dimension growth, γ , which is estimated from electron micrographs. The effective conductivity along the diamond films increases rapidly with increasing layer thickness due both to the decreasing imperfection concentration and to the reduced importance of phonon scattering on layer boundaries. Phonon scattering on layer boundaries is particularly important

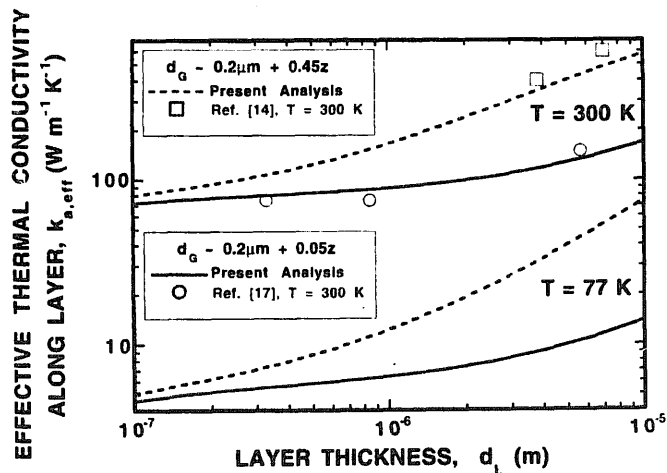


Fig. 6. Lateral thermal conductivity along thin diamond layers at room temperature and 77 K.

at 77 K due to the long free paths in bulk samples at this temperature. This effect causes the conductivity to be orders of magnitude smaller than the values prevailing in thick diamond plates at that temperature.

Fig. 7 illustrates that fixing the grain-boundary scattering strength, which is the approach for Fig. 6, is not successful for modeling all of the thin layers whose conductivities have been measured near room temperature. The data exhibit more scatter and a weaker dependence of the conductivity on the film thickness, suggesting a large sensitivity of the lateral thermal conductivity on the deposition details. The data reported by Verhoeven et al. [12] for the layers with highly-oriented and heteroepitaxial grains show a large degree of anisotropy, with in-plane conductivity being smaller by an order of magnitude than out-of-plane conductivity. One method for interpreting the large variation of the resistance is to assume a local in-plane thermal conductivity that does not depend on z and to introduce an intergrain boundary resistance. For steady state heat conduction and for transient conduction with thermal diffusion lengths much greater than the average grain size, the in-plane conductivity can be approximated

$$\frac{d_G}{k_a} \cong \frac{d_G}{k_{ig}} + R_i \quad (7)$$

where d_G is average grain dimension, k_a and k_{ig} are total effective and intragrain values of in-plane conductivities, respectively, and R_i is the thermal resistance at grain boundaries. This intergrain boundary resistance is particularly helpful in explaining the strong anisotropy measured by Verhoeven et al. [12]. These measurements showed a large anisotropy of a thermal conductivity for highly oriented films. The values of the resistance

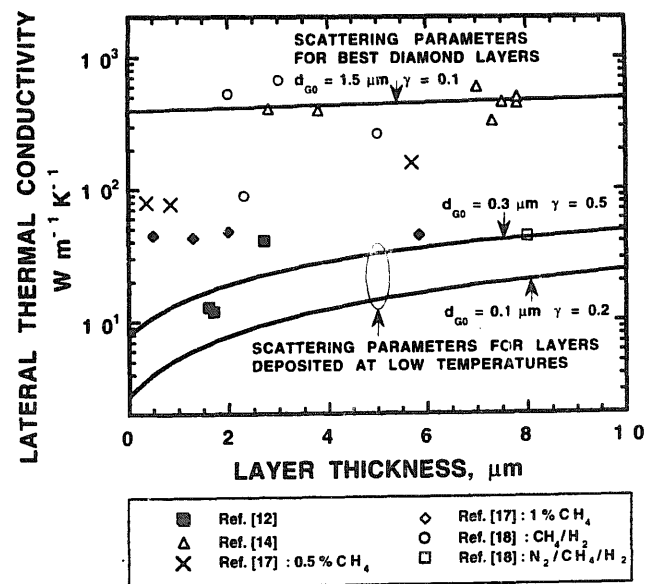


Fig. 7. Lateral thermal conductivity of diamond layers thinner than 10 μm.

between the grains are estimated using Eq. (7) to be of the order of $10^{-8} \text{ m}^2 \text{ K}^{-1} \text{ W}^{-1}$ for layers deposited near both 500 and 800 °C.

This observation about R_i compares well with the observations of Verhoeven et al. [24] for much thicker diamond films deposited near 800 °C. These data were taken using transient thermal gratings with a small spatial period of heat source compared to the average grain dimension. The measurements on the 170 μm thick samples with a characteristic grain dimension of $d_G = 28 \mu\text{m}$ revealed a strong position dependence of the local in-plane thermal diffusivity. The diffusivity varied by as much as 35% depending on the distance from the boundary of the chosen crystal. The highest value of thermal conductivity calculated from the diffusivity was found to be $1700 \text{ W m}^{-1} \text{ K}^{-1}$, and is consistent with the predictions of $1780 \text{ W m}^{-1} \text{ K}^{-1}$ for the grain size of 28 μm calculated using the model described in the Section 2.4. By introducing a thermal resistance between grains, the same work [24] determined this resistance to be $8.5 \times 10^{-9} \text{ m}^2 \text{ K W}^{-1}$ which is consistent with our estimate here for thinner layers, suggesting that the intergrain thermal resistance is weakly dependent on the distance from the boundary. The limitations set by the smallest achievable spatial period of heat deposition in the transient thermal grating method do not allow direct measurements of the local in-plane diffusivity for thin layers with grain sizes comparable to or less than 1 μm .

3. Applications and impact of micron-scale diamond layers in microdevices

3.1. Silicon-on-diamond

A buried layer of electrically-insulating material allows significant improvements in the performance of electronic devices. Silicon-on-insulator technology realizes a silicon overlayer of thickness between about 0.03 and 20 μm , depending on the application, directly above a dielectric thin film or substrate [25]. For fast logic circuits, the presence of the dielectric reduces the effective electrical capacitance of transistors and interconnects and makes possible higher clock frequencies. For high-power circuits, the buried dielectric makes possible fully-isolated semiconducting islands that facilitate integration, in particular with low-voltage logic. The most mature SOI technology uses a buried amorphous silicon dioxide layer of thickness between 0.2 and 2 μm within a silicon substrate. Amorphous silicon dioxide has a very low thermal conductivity, between 0.8 and $1.4 \text{ W m}^{-1} \text{ K}^{-1}$ depending on the fabrication process [26,27]. This results in a thermal resistance between the device and the silicon substrate that strongly increases the temperature rise in SOI transistors and can decrease the median time to failure of transistor-interconnect

contacts [28,29]. The self heating problem for SOI is most important for applications in which devices must withstand brief, high-power pulses, such as those occurring in a control system or in devices protecting logic circuits from electrostatic discharge (ESD) failure.

A potential solution is to fabricate a composite substrate using diamond as the buried insulator, which promises a high electrical resistance and breakdown voltage together with a very low resistance to heat conduction. There are several approaches for fabricating silicon-on-diamond (SOD) substrates. Ravi and Landstrass [30] developed bond and etch-back technology for making the composite silicon-on-diamond (BESOD) substrate shown in Fig. 8. The surface of a silicon wafer is doped with boron. An epitaxial silicon layer is grown on the boron-doped surface, followed by deposition of a polycrystalline CVD diamond film. The diamond is covered by a polycrystalline silicon layer and bonded to another silicon wafer after polishing. The original single-crystal silicon wafer is etched away except for the thin layer containing boron, which serves as an etchant stop and is subsequently removed. Transistors are fabricated from the remaining epitaxial silicon overlayer. This process has the disadvantage that the active silicon region serves as the deposition surface for the diamond and may be damaged by the nucleation process. The diamond nearest the silicon has the poorest microstructure, which inhibits conduction cooling from the silicon into the diamond. Additional methods that may prove promising make use of zone-melt recrystallization (ZMRSOD) of polysilicon [31,32] and the combined lateral and vertical growth of crystalline silicon [33–35] through etched windows in the diamond.

To investigate the impact of replacing silicon dioxide by diamond within an SOI circuit, the temperature rise due to pulsed heating is calculated for the case of an SOD transistor. The calculations use the closed-form solution to the transient, three-dimensional thermal-conduction equation for the geometry in Fig. 9 with a 0.5 μm thick silicon overlayer and 1 μm buried insulating layer. For the case of the BESOD sample, the calculations consider 5 μm of polycrystalline silicon beneath the insulating layer. The dimensions L_x and L_y describe

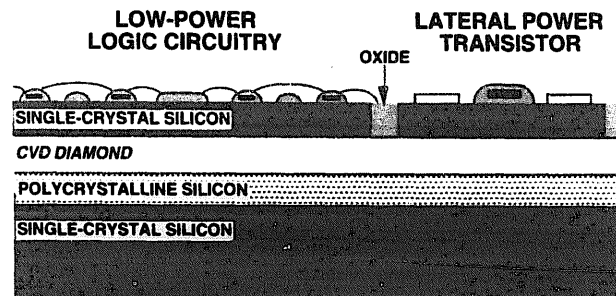


Fig. 8. Schematic of a silicon-on-diamond smart power circuit fabricated using technology developed by Annamalai et al. [31].

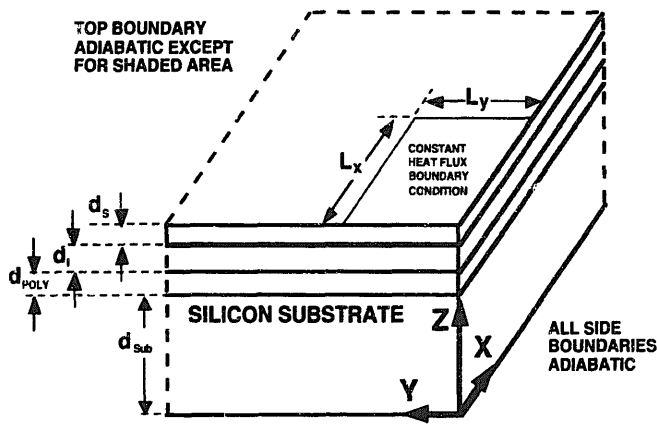


Fig. 9. Geometry used for predicting the temperature rise in devices fabricated on SOD wafers compared with conventional SOI wafers containing silicon dioxide.

the lateral extent of the power device and are each 500 μm . Fig. 10 shows the predicted impact on the peak temperature rise as a function of the duration of the heating pulse. For these calculations, the diamond effective thermal conductivity in the direction normal to layers is assumed to be $110 \text{ W m}^{-1} \text{ K}^{-1}$, which results from the model in Section 2.3 applied for the diamond layers deposited at high temperatures with a minimum grain dimension $d_{G0}=100 \text{ nm}$ and a grain growth parameter $\gamma=0.5$. Fig. 10 shows that bringing diamond within micrometers of the active region can strongly reduce the temperature rise during the pulsed heating compared to that occurring in conventional SOI wafers. The temperature rise in the device is proportional to the thermal mass heated during the pulse, which for brief pulses is governed by heat diffusion within the layers closest to the device. The benefit is greatest for pulsed heating of duration comparable to the heat diffusion time normal to the buried oxide, which is of the order of a microsecond for the layer of thickness near 1 μm considered here. In the case of much briefer pulses, the temperature reduction resulting from use of diamond is

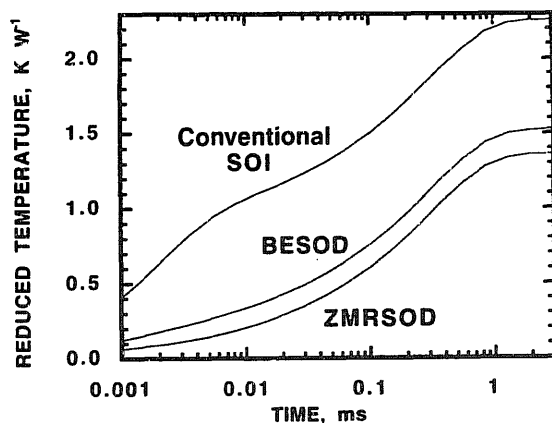


Fig. 10. Temperature rise per unit power of devices fabricated on SOD wafers compared those made with conventional SOI wafers.

approximately proportional to ratio of the thermal diffusion lengths in diamond and oxide multiplied by the ratio of the volumetric heat capacitances. Fig. 10 shows that considerable benefit can be obtained even through the use of a diamond layer with thermal conductivity comparable to that of silicon, which Section 2.4 showed is typical in films grown at low temperatures. This may allow production of SOD wafers free from warpage, which is a result of high deposition temperatures, without sacrificing the improved thermal performance of devices fabricated on such wafers. The performance improvement for SOD is governed mainly by the vertical conduction properties of the diamond layer.

Thermal conduction in composite diamond/silicon substrates was studied by Edholm et al. [36], who made diodes from a silicon overlayer on diamond. The starting material was 600 μm thick SOI wafer with 10 μm silicon overlayer on 0.5 μm buried oxide. The diodes had a width of 10 μm and a 60 μm lateral spacing in an array. The fabrication process etched a window through the silicon substrate, after which a 5 μm diamond layer was deposited from the back side. A heating pulse with of 100 μs duration was induced in the heating diode. Temperature measurements were performed using a neighboring diode by monitoring the change in the reverse avalanche breakdown voltage. The authors determined from the data that the lateral conductivity of the diamond was about an order of magnitude less than that of bulk diamond, which is consistent with the layer conductivities discussed in Section 2. The authors determined that the use of a copper heat sink, which was electroplated to the back of the diamond, resulted in a total junction-to-ambient thermal resistance that was smaller by a factor of two than that for a reference SOI wafer. This measurement approach provides limited information, however, since the effect of the reduced thermal resistance in the diamond is greatest at the heat source. At the neighboring diodes, which were separated from the active device by 60 and 180 μm , the contribution of diamond to lateral heat flow may be overwhelmed by that due to the thick copper heat sink. Future measurements determining the impact of using diamond instead of silicon dioxide must use heating and thermometry at the same location, since this will yield data most sensitive to the thermal properties of the buried insulator.

New attachment technologies promise to make possible composite substrates containing passive diamond and active gallium-arsenide devices, for example, laser diodes and microwave-frequency transistors. Thin gallium arsenide layers can be removed from bulk gallium arsenide substrates using a sacrificial aluminum arsenide release layer. A membrane resulting from this process was attached to a diamond substrate without an interfacial material [37]. Transmission electron micrographs

of the interface of gallium arsenide attached to silicon using the same technology show an amorphous interfacial layer of thickness near 100 Å. The thermal resistance due to an amorphous layer of this thickness is probably quite small, of the order of $10^{-8} \text{ m}^2 \text{ K W}^{-1}$ at room temperature [24]. If this technology can be mastered, it may prove possible to fabricate very compact optoelectronic circuits through enhanced conduction in diamond. Although this application is not strictly the same as the other classes of applications in Table 1, it is included here because it brings diamond within micrometers of the active region.

3.2. Diamond passivation

The low electrical conductivity of diamond combined with its high thermal conductivity makes it very attractive as a passivation material. The feasibility of this application has been receiving more attention after recent advances in diamond deposition [22,23], which reduced the substrate temperature below 500 °C while maintaining diamond material with reasonable stoichiometric and phase purity. The low deposition temperatures are approaching the requirements for compatibility with integrated circuit structures containing aluminum and silicon. The passivation of interconnects and power devices will be feasible if the damage to underlying layers during the pretreatment for nucleation is minimized. The electron micrograph in Fig. 1 illustrates that step coverage can be achieved using diamond. The microstructure is favorable to heat flow out of the line with grains having orientation normal to the surface of coated line in all directions. From a thermal design perspective, the most benefit from the use of diamond as a passivation material can be gained during brief pulses of heating typical during the switching operation of the devices or ESD. The passivation layer is most effective at reducing transient temperatures of interconnects or power devices if the volume of passive material heated during the pulse is comparable with or greater than the volume of the active region. This requirement sets a condition on the acceptable thermal diffusivity of the material.

There are reports in the literature assessing possible benefits from the use of diamond-like-carbon passivation. Szmidt [38] used thin layers of diamond-like-carbon (DLC) as passivation coatings for power bipolar transistors and observed an improvement in device operation, which was manifested by a reduction of the base-emitter leakage current. It is not clear if the improvement in the electrical behavior was due to the reduced device temperature. Frischoltz et al. [39] studied the effects of DLC passivation on the breakdown voltage of a p–n junction and observed that no breakdown occurred even with the increase of the applied voltage to more than twice the breakdown voltage of the unpass-

sivated junction. The improvements in the device operation motivate further research to be of importance in assessing this potential diamond application. The DLC layers in the studies of Szmidt [38] and Frischoltz [39] must be distinguished from the relatively high-quality diamond discussed elsewhere in this manuscript, which have thermal conductivities much larger than those of DLC layers [46].

This manuscript aims to determine if the quality of the low-temperature deposited diamond can be satisfactory for reducing the temperature rise in devices and interconnects subjected to brief heating pulses. Figs. 11 and 12 predict the relative reduction of the temperature rise of a pulse-heated interconnect compared to that in

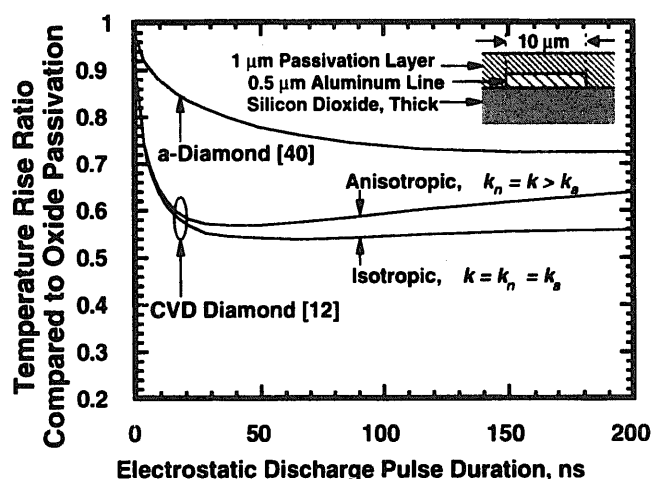


Fig. 11. Ratio of the temperature rise in a diamond-passivated top-level interconnect to the temperature rise in an interconnect passivated using silicon dioxide. The lateral thermal conductivity in the anisotropic case is reduced by a factor of 10 from that in the isotropic case. The width of the interconnect is 10 μm .

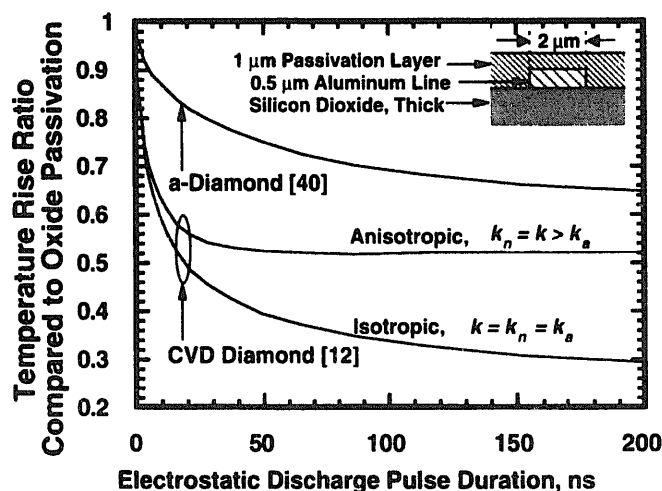


Fig. 12. Ratio of the temperature rise in a diamond-passivated top-level interconnect to the temperature rise in an interconnect passivated using silicon dioxide. The lateral thermal conductivity in the anisotropic case is reduced by a factor of 10 from that in the isotropic case. The width of interconnect is 2 μm .

an interconnect passivated by silicon dioxide for three values of thermal conductivity. The thermal conductivity value of $10 \text{ W m}^{-1} \text{ K}^{-1}$ is typical of nanocrystalline diamond conductivities reported in the literature [40]. Verhoeven et al. [11] reported effective thermal conductivities normal to thin diamond layers deposited on silicon at low temperatures close to $100 \text{ W m}^{-1} \text{ K}^{-1}$, while the lateral property can be an order of magnitude lower [12]. Data are needed to determine if similar conductivity values will be possible in layers deposited on metals. For the case of diamond layers nucleated using mechanical pre-treatment, it is reasonable to expect that the thermal conductivity of diamond on polysilicon to be similar to that of diamond on silicon. The orientation and boundaries of grains in polysilicon may not alter significantly microstructure induced by the pretreatment. The predictions neglect thermal resistance at the boundary. Figs. 11 and 12 show that the temperature rise can be significantly reduced compared to that for the case of silicon dioxide passivation. These figures also demonstrate the impact of anisotropic thermal conductivity on the transient temperature rise in the interconnect. For the interconnect with smaller width, the lateral heat spreading in the passivation layer is more pronounced compared to a wider interconnect. This results in a more sensitive dependence of the temperature rise on the layer anisotropy. Diamond passivation can also prove to be very beneficial in many other applications, including SOI, SiGe and GaAs devices, in which the local temperature rise is augmented by buried interfaces and disordered regions. The calculations presented here most closely simulate transient heating during ESD, which occurs with timescale shorter than 100 ns and results in catastrophic failure due to melting of devices and interconnects [41,42]. Since the calculations performed here are based on thermal properties measured in layers fabricated at temperatures compatible with IC technology, Figs. 11 and 12 provide reasonable estimates of the impact of diamond passivation on temperature fields during pulse heating of interconnects. The reduction in temperature rise of diamond passivated interconnects compared to oxide-passivated interconnects can be significant, >40% for polycrystalline CVD diamond and ca 30% for amorphous diamond after a 100 ns pulse for the typical power-line geometry shown in Fig. 11. As seen from Fig. 12, the effect of diamond passivation on narrower interconnects is more significant due to the increased importance of lateral heat spreading. However, achieving these estimated reductions in temperature rise requires further research on diamond deposition techniques, particularly for deposition on non-planar geometries.

3.3. Microfabricated thermal sensors

Thermal sensors detect changes in a property or a flux in a system by measuring changes in temperature,

often using the temperature dependence of the electrical resistance of a metal or superconducting bridge. Examples include bolometers, which detect changes in the radiation flux incident on an absorbing element [43], and anemometers, which measure the velocity of liquid motion around a wire or bridge [44]. The time constant and the responsivity of a thermal sensor are governed by the specific heats and thermal conductivities of the materials in the sensor and surrounding structure. The high thermal conductivity of diamond and its relatively low specific heat can be used to dramatically reduce the time constant of thermal sensors. In some cases, this can be achieved without diminishing the responsivity. The MEMS community has proposed or developed a variety of thermal sensors that include diamond regions. These have included fast superconductor radiation detectors [45], thin-bridge flow-velocity sensors [46] and high-temperature thermistors [47–49].

Roppel et al. [46] investigated the impact of the use of diamond on the time constant of the anemometer, which was developed for use in liquid nitrogen at temperatures <77 K. Etching was used to suspend a bridge between heating and temperature-sensing electrical resistors made of doped silicon. For a given heater power, the steady-state temperature achieved at the temperature-sensing bridge decreased with increasing flow velocity due to the improved convection to the fluid from the bridge. Predictions indicated that the use of diamond rather than silicon could reduce the time constant of the sensor by >50% to ca 72 ms. In practice, the authors found that the sensor containing diamond responded more quickly, but that the meaningful response was overshadowed by a relatively large temperature rise that occurred at long timescales due to heating in the substrate. This problem could be overcome through the use of an oscillating current in the heating resistor with period comparable to the timescale for conduction along the suspended diamond bridge. The voltage induced by a steady-state current along the temperature-sensing bridge can then be monitored using a lock-in amplifier. The amplitude and phase shift of the response will be very sensitive to the fluid velocity.

The time constant of many thermal sensors is well approximated by the ratio C/G , where C is the total heat capacity of the temperature-sensing resistor and the supporting structure with which it is in direct contact, and G is thermal conductance linking this heat capacitance to a body whose temperature varies little with time [43]. In this approximation, the response of the bolometer due to a given change in radiation power increases with decreasing values of the conductance. The engineering of fast thermal sensors must compromise between the need for a short time constant, for which a large conductance must be targeted, and the need for a large responsivity, which requires a low value of the conductance. This compromise is assisted through

the minimization of C , which can reduce the time constant without influencing the responsivity of the sensor. In bolometers operated at frequencies considerably larger than the inverse of the time constant, the responsivity increases with decreasing C [50], making this approach to diminishing the time constant especially helpful. The very low specific heat of diamond at low temperatures makes it an attractive material for minimizing the heat capacitance of the passive regions in a bolometer. At temperatures small compared to the Debye temperature of a dielectric or semiconducting solid, the specific heat per unit volume at the temperature T is proportional to $nk_B(T/\theta)^3$, where n is the atomic number density and k_B is the Boltzmann constant. The Debye temperature θ of diamond, ca 2230 K, is more than three times larger than that of silicon, silicon dioxide, and most other materials in electronic microstructures. The large difference in Debye temperatures yields a specific heat per unit volume in diamond at low temperatures that is very small. Section 2 showed that the thermal conductivity of diamond layers can depend strongly on layer thickness and on the details of the deposition process. The specific heat per unit volume of the diamond layer is not very sensitive to imperfection concentrations in the material. It may prove possible to tailor the deposition of a passive diamond layer in a bolometer structure to yield a conductivity that results in a targeted time constant and responsivity.

This can be demonstrated by considering a microfabricated bolometer similar to that developed by Verghese et al. [51], who suspended a bridge of the high- T_c superconductor $\text{YBa}_2\text{Cu}_3\text{O}_7$ on a dielectric bridge above a silicon substrate. The bolometer was operated near the transition temperature of the superconductor, where its electrical resistance depends very strongly on temperature. The bolometer of Verghese et al. [51] was designed to yield a very high responsivity to incoming radiation by minimizing the thermal conductance to the substrate. This motivated the use of an amorphous silicon nitride bridge, which had a very low thermal conductivity and a small cross-sectional area. The heat capacity of the bolometer was governed by that of the supporting silicon nitride and the superconducting and metal layers. If diamond is used rather than silicon nitride for the membrane material, the heat capacitance of the passive supporting bridge could be strongly reduced. Fig. 6 shows that the effective in-plane thermal conductivity at cryogenic temperatures along thin diamond layers can also be very small, even comparable to that of silicon nitride, such that the responsivity of the bolometer would not be strongly reduced. While the fabrication of a high- T_c superconducting bolometer on a diamond membrane represents a major challenge, progress on the deposition of $\text{YBa}_2\text{Cu}_3\text{O}_7$ on diamond using very thin buffer layers is promising [52,53].

The large bandgap of diamond, 5.45 eV, makes the

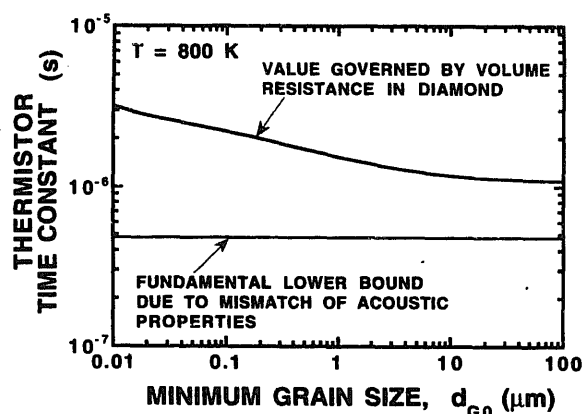


Fig. 13. Time constant of a diamond thermistor operating at high temperature as a function of the diamond grain size at the interface with the substrate.

material in doped form suitable for use in a thermistor structures at relatively high temperatures [47–49]. The diamond electrical conductivity is increased through doping with boron, whose concentration influences the thermistor sensitivity to temperature variation. Although this device is using diamond as an active material, it is included in the present manuscript in an effort to make the microsensor discussion as complete as possible. A typical thermistor structure is fabricated by depositing ca 10 nm of intrinsic polycrystalline diamond on a metal surface in a MEMS structure. This is followed by deposition of roughly 1 μm of boron-doped diamond, whose relatively large grain dimensions are essential to achieve reasonable sensitivity of the electrical conductivity to temperature variation. It is useful to know the timescale of the most rapid fluctuations that can be detected using this thermistor. Because the metal and the diamond far from the interface will both have high thermal conductivities, the time constant will be governed by the thermal resistance for conduction from diamond into the metal. The time constant is estimated as RdC , where R is thermal resistance for conduction from the diamond and d and C are the thickness and specific heat per unit volume of the diamond. Fig. 13 plots this estimate of the thermistor time constant as a function of the grain dimension at the diamond–silicon boundary, d_{G0} . The time constant decreases with increasing values of d_{G0} because the effective boundary resistance decreases. Fig. 13 also estimates the fundamental lower bound for the time constant using a value of R equal to the diffuse mismatch resistance at a diamond–copper boundary. Fig. 13 illustrates that imperfection in diamond near its boundary with other materials can strongly influence the time constant of thermistors.

4. Conclusions and recommendations

There remain several important tasks for thermal analysis of micron-scale diamond layers and microde-

vices containing diamond. There is a need for thermal conductivity and boundary resistance data for diamond layers deposited on metals and for non-flat diamond step-coverage regions such as those shown in Fig. 1. To establish confidence in the predictions provided in Section 3, there is also a need for thermal characterization experiments on active devices showing the impact of improved thermal conduction in diamond on temperature fields and device current–voltage characteristics. Although Section 2.4 showed that the thermal conductivities of diamond layers deposited near 500 °C are considerably lower than those of bulk diamond, they may still be orders of magnitude larger than those of competing passive materials of similar thickness. To clearly examine this issue, there is a need for accurate thermal property measurements of thin films of the competing materials in Table 1, including low-temperature deposited silicon dioxide, silicon nitride and even aluminum nitride films. The thermal conductivities of these relatively disordered layers will almost certainly be much smaller than those of bulk materials with the same stoichiometry.

The main goals of this review are to quantify the implications for thermal design of the second class of diamond layer applications described in Table 1. This review has calculated the temperature fields in devices using micron-scale diamond layers, in most cases considering values of the thermal conductivity for layers fabricated at temperatures compatible with the given microdevice technology. For the cases of SOI devices, low-temperature sensors, and power transmitting interconnects that must withstand rapid electrical stressing, this review shows that the use of diamond thin films offers significant improvements in thermal conduction cooling compared to the use of more conventional silicon dioxide and nitride. However, this review has made no attempt to detail the fabrication and cost challenges associated with integrating diamond deposition with fabrication of specific microdevices. Although deposition technology has made substantial progress in the areas of growth temperature and nucleation on nonflat and nonhomogeneous surfaces, the technology must still make much progress before a convincing case can be made for integration with IC technology. For this reason, an immediate challenge for the materials research community is to provide a quantitative assessment of the prospects for achieving deposition compatibility.

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