Micromachined Jets for Liquid Impingement Cooling of VLSI Chips

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***Abstract*—Two-phase microjet impingement cooling is a potential solution for removing heat from high-power VLSI chips. Arrays of microjets promise to achieve more uniform chip temperatures and very high heat transfer coefficients. This paper presents the design and fabrication of single-jets and multijet arrays with circular orifice diameters ranging from 40 to 76 μm, as well as integrated heater and temperature sensor test devices. The performance of the microjet heat sinks is studied using the integrated heater device as well as an industry standard 1 cm^2 thermal test chip. For single-phase, the silicon temperature distribution data are consistent with a model accounting for silicon conduction and fluid advection using convection coefficients in the range from 0.072 to 4.4 W/cm^{2}K. For two-phase, the experimental results show a heat removal of up to 90 W on a 1 cm^2 heated area using a four-jet array with 76 μm diameter orifices at a flowrate of 8 ml/min with a temperature rise of 100 °C. The data indicate convection coefficients are not significantly different from coefficients for pool boiling, which motivates future work on optimizing flowrates and flow regimes. These microjet heat sinks are intended for eventual integration into a closed-loop electroosmotically pumped cooling system. [1186]**

***Index Terms*—Heat sink, integrated circuit packaging, jet impingement, microjet, two-phase cooling.**

I. Introduction

THE rapidly increasing heat generation rates in very large scale integrated (VLSI) circuits pose severe thermal challenges for the semiconductor industry in the future. Heat fluxes of over 60 W/cm^2 need to be removed from high performance chips in the next five years as predicted by the International Technology Roadmap for Semiconductors (ITRS) [1]. Conventional cooling methods such as forced air convective cooling are impractical at these high heat flux levels due to the large volume and weight associated with metal fin-array heat sinks. These large heat removal requirements are motivating research on a broad variety of advanced thermal management solutions.

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Micromachined heat sinks including microchannels and microjets occupy a small volume on the chip backside and promise low thermal resistances. Tuckerman and Pease demonstrated heat removal of 790 W/cm^2 with a water flowrate of 516 ml/min using single-phase liquid convection in microchannels [2], and this work led to extensive research focusing on microchannel heat sinks with single-phase and two-phase cooling. Bowers *et al.* showed that two-phase microchannels can remove over 200 W/cm^2 with flowrates of less than 65 ml/min and pressure drops of less than 5 psi [3]. Other microchannel studies include two-phase heat transfer modeling using the homogeneous flow assumption [4], and understanding nucleation mechanisms and phase change phenomena [5]–[8].

Micromachined heat sinks that direct liquid jets at the surface of a chip have recently received attention because they offer several advantages over microchannels and other cooling methods. These advantages include the fact that the thin liquid boundary layer just outside of the impingement region promises higher heat removal rates, impingement directly onto the backside of the chip eliminates the conduction resistances in the layers associated with the packaging, and a jet array helps achieve uniform cooling on the chip surface. In addition, the fluid impingement with a carefully located single jet can provide highly localized cooling of hotspots on chips with nonuniform heat generation. There are problems, though, including stability of the jet for differing flowrates and fluid recovery.

There has been much experimental work on free liquid jet convection with macroscale jets with orifice diameters larger than 1 mm and $2000 < \mathrm{Re_d} < 51\,000$, where $\mathrm{Re_d}$, the Reynolds number, is based on the orifice diameter [9]–[12]. Stagnation Nusselt numbers were found to be constant for ratios of radial distance to orifice diameter of less than 0.75 and relatively unaffected by orifice to plate spacings [9], [10]. Single-phase submerged and confined jets show similar heat transfer characteristics to free jets for $\mathrm{Re_d} < 4000$ [13]. Womac *et al.* found optimal orifice to plate separations of less than 4 to achieve the highest heat transfer coefficient particularly for $\mathrm{Re_d} \leq 4000$ [11], while Elison *et al.* reported the stagnation Nusselt number to be independent of the orifice to plate separation for $\mathrm{Re_d} \leq 1500$ [9]. Garimella *et al.* reported experimentally determined heat transfer coefficients as high as 6 W/cm^{2}K for $\mathrm{Re_d} = 23\,000$ [14].

Boiling jet impingement can achieve significantly higher heat removal rates by utilizing the latent heat of vaporization. Jet impingement boiling characteristics which include subcooling, surface condition, and velocity effects were experimentally examined for jets with orifice diameters greater

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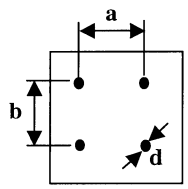
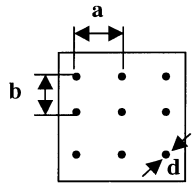
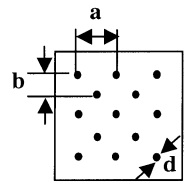
TABLE I
THE GEOMETRY AND CONFIGURATION FOR THE THREE DIFFERENT JET ARRAYS TESTED ON A 1 cm^2 HEATER. THE JETS ARE 300 μm IN LENGTH

		
4-jet array	9-jet array	13-jet array
d = 70-76 μm	d = 50 μm	d = 40 μm
a = 5 mm	a = 3.5 mm	a = 4 mm
b = 5 mm	b = 3.5 mm	b = 2 mm

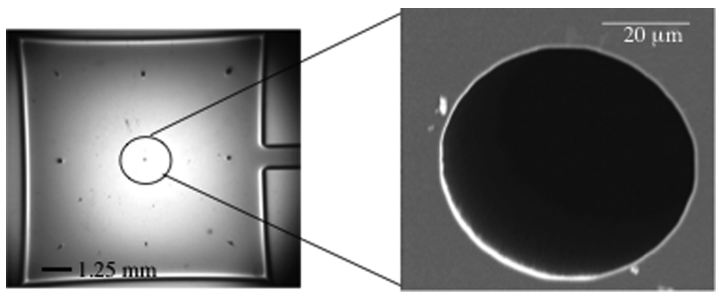


Fig. 1. Picture of a nine-jet array and a SEM of the associated 50 μm orifices.

than 1 mm [15]–[17]. These studies show that convective coefficients were relatively insensitive during fully developed boiling, where convection is dominated by the mixing induced by bubbles leaving the surface. However, fluid temperature and velocity have a significant impact on partial nucleate boiling, where the bubble population is typically low. In fully developed boiling, Wolf *et al.* reported a heat flux removal of over 400 W/cm^2 with a wall superheat of 30 °C–40 °C and flowrate of 1.2×10^5 ml/min [17].

While the performance of macroscale jet impingement is promising, the associated flowrates are not practical for an integrated VLSI chip cooling system due to the necessary pumping capability and the size constraints of the system. Past research on microjet impingement cooling focused on using air as the working fluid. Relatively low heat flux removal rates (<20 W/cm^2) have been demonstrated with air impingement due to the limitation of single-phase heat transfer. Single-jets and multijet slot and nozzle arrays with orifice diameters ranging from 50 to 3000 μm made of glass and silicon were characterized [18]–[21], including integration with heat sink modules [19] and actuation by magnetically driven membranes [18]. More recently, Leland *et al.* fabricated arrays of 221 jets with orifice diameters of 277 μm and demonstrated a removal of 15 W/cm^2 with a temperature rise of 50 °C in a confined geometry [22]. Few studies have focused on microscale liquid impingement. Heffington *et al.* studied Vibration Induced Droplet Cooling (VIDA) where a piezoelectric disk atomizes water droplets of diameters 70–800 μm. Removal of 200 W/cm^2 heat flux with a 100 °C temperature rise was demonstrated with a chilled water heat sink as the external heat removal device [23]. In our past work, we characterized liquid jets with single orifice diameters less than 50 μm and have removed 40 W/cm^2 heat flux with a water flowrate of 2–3.5 ml/min with an 80 °C temperature rise [24].

In this work, we experimentally examine the performance of single-jets and multi-jet arrays with orifice diameters ranging from 40 μm to 76 μm in a confined geometry for liquid-phase and two-phase heat transfer. The cooling effectiveness of liquid jets is studied using integrated heater and thermometer devices and then tested using an Intel thermal test board. The microjet heat sinks are designed for use in the integration of a closed-loop electroosmotically pumped cooling system.

II. DESIGN

Silicon microjets were fabricated with circular orifices ranging from 40 μm to 76 μm in diameter and are 300 μm in length. Three different multi-jet array configurations were chosen based on the necessary flowrates and associated pressure drops for jet formation in accordance with previous work [24], to study the temperature profile on a constant heat flux surface. The design of the jet arrays was also limited by specifications of the latest electroosmotic pumps, which provide flowrates up to 33 ml/min and pressure drops of 20 psi [25], in order to integrate these heat sinks into a closed-loop pumped system in the future. With these parameters, optimal array configurations were determined to be four of 70 μm–76 μm, nine of 50 μm, and thirteen of 40 μm diameter jets, as shown in Table I. A scanning electron micrograph (SEM) of the 50 μm jet orifice is shown in Fig. 1.

The integrated heater test chip, designed to emulate a high-power IC chip, has a 1 cm^2 heated area and seven temperature sensors along the centerline as shown in Fig. 2. These sensors are spaced 1 mm apart and measure a one-dimensional (1-D) temperature profile. There is a 200-μm-deep reservoir on

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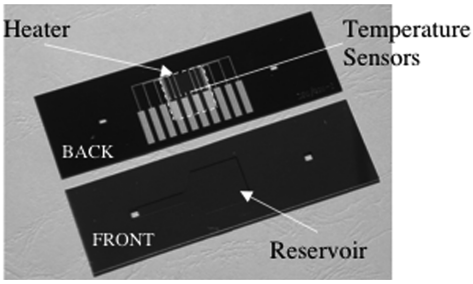

Fig. 2. Picture of a fabricated heater device emulating a high-power IC. The reservoir on the front side is 200 μm in depth and serves as the impingement plane for the jets. The back side of the chip shows a 1 cm^2 heater and seven calibrated temperature sensors along the centerline.

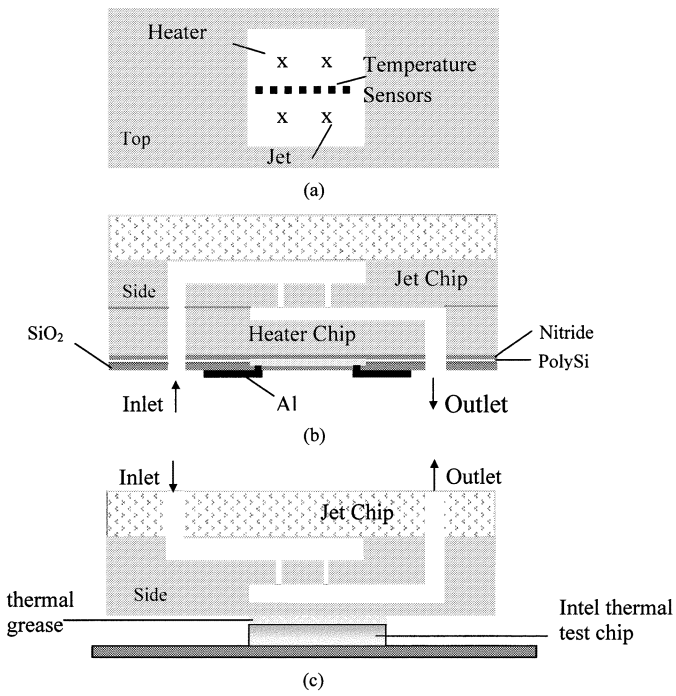

Fig. 3. Schematics of the test device configurations. (a) Top view of the bonded jet and heater test device. The crosses on the top view show the configuration for a four-jet array with respect to the placement of the temperature sensors. (b) Cross-sectional view of the bonded jet and heater test device. The reservoir collects and recirculates the impinging water. (c) Cross-sectional view of a jet chip placed on top of the Intel thermal test chip board. A layer of thermal grease is used to achieve good thermal contact.

the front side of the chip to collect the impinging water. The reservoir depth was chosen based on past jet literature, which reports that an optimal orifice and reservoir spacing for heat transfer is 2–4 times the jet diameter [11]. This consideration ensures that the impingement occurs within the region of the potential core of the jet, where the velocity profile is uniform.

Two different test configurations were used in the experiments, one consisting of a set of fabricated jet and heater chips, and the other consisting of fabricated jet chips placed on top of an Intel thermal test board. The combination of the microjet and the heater test chip, shown in Fig. 3(b), creates a confined geometry device. The jets are fully enclosed by a reservoir on the front side of the heater chip. The fluid enters the defined inlet and moves toward the top reservoir into the jet orifices. Once the pressure overcomes the droplet surface tension, the jets form and impinge onto the bottom heated chip surface. The heated fluid then is collected at the bottom reservoir and flows toward the outlet. This confinement prevents electrical shorting and allows for fluidic recapture intended for the eventual integration into a closed-loop cooling system. As a result of this confined geometry, this heat transfer study consists of confined, submerged microjet impingement, where the liquid from the jet issues into a reservoir containing the same liquid. Furthermore, the confinement from the side wall creates an additional flow component toward the outlet. The second configuration for the microjet device design used for testing the 100 W Intel thermal test board is shown in Fig. 3(c). The heater and temperature sensors are provided on the board so the confined geometry cooling device consists only of the jet chip and a reservoir chip, with no fabricated heater or temperature sensors.

III. Fabrication

Standard silicon micromachining processes, similar to those by Zhang *et al.* [7], were used to fabricate the jet and heater test structures. The jet and heater devices are fabricated separately and are described briefly below. For the jet structures, the orifices are first made into single crystal silicon substrates using Deep Reactive Ion Enhanced (DRIE) etching. Then, on the back side, a 1 cm^2 reservoir and an inlet hole are etched also using DRIE. Finally, a Pyrex 7740 glass wafer is anodically bonded to the silicon substrate to seal the inlet and reservoir. To fabricate the heater test devices, a 1 cm^2 reservoir and outlet hole are first plasma etched into silicon N-type substrates. An insulating nitride layer and a polysilicon layer are deposited, as shown in Fig. 3(a). The polysilicon is then doped with boron with a 1×10^{15}/cm^2 dose and 60 keV energy level to define the resistors for the heater and seven thermometers. An oxidation and annealing process repairs the implantation damage and forms the resistors. Finally, aluminum is deposited to make electrical contacts to the resistors. To make confined geometry test devices, the jet chip and the heater chip are bonded together with 5-min cure epoxy (Devcon, MA).

Polysilicon doped temperature sensors are used to examine the temperature profile. Through calibration, the surface temperature of the heater can be monitored at various locations with the array of temperature sensors located along the centerline. The calibration requires placement of the heater device in a convection oven where the resistance of the sensor is monitored as the oven temperature is increased. The resistance of the heater is 500 Ω and each thermometer is 6.7 kΩ at room temperature. An example of the temperature sensor calibration is shown in Fig. 4. Because the change in resistance over the temperature range is nonlinear, the temperature sensitivity ranges from -6 Ω/°C to -20 Ω/°C.

IV. Experimental Setup

Fig. 5 shows a schematic of the experimental setup used for the measurements reported in this work. A syringe pump (Ph.D. 2000, Harvard Apparatus, MA) delivers deionized (DI) water to the inlet of the jet device. Water is selected for the experiments for its high heat capacity (4179 J/kgK), latent heat of vaporization (2438 kJ/kg), and simplicity. A pressure sensor (MSP400, Measurement Specialties, Inc., PA) near the inlet measures the

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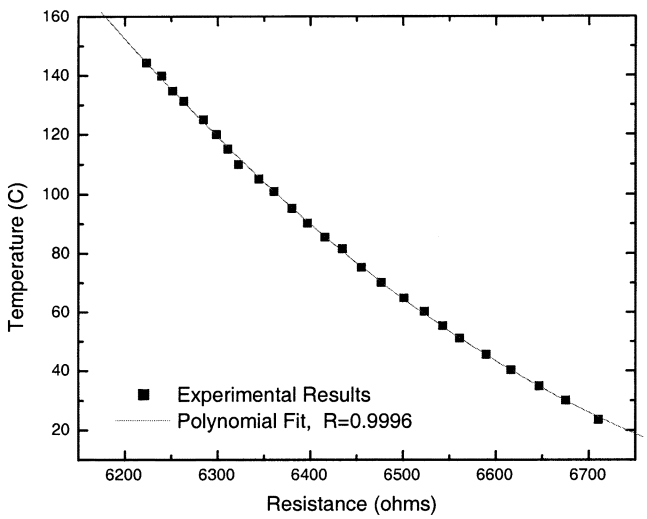

Fig. 4. Calibration results and polynomial fitting curve for a typical temperature sensor. The temperature sensitivity ranges from $-6\ \Omega/°\mathrm{C}$ to $-20\ \Omega/°\mathrm{C}$. Uncertainty in the calibration is estimated to be 0.2%.

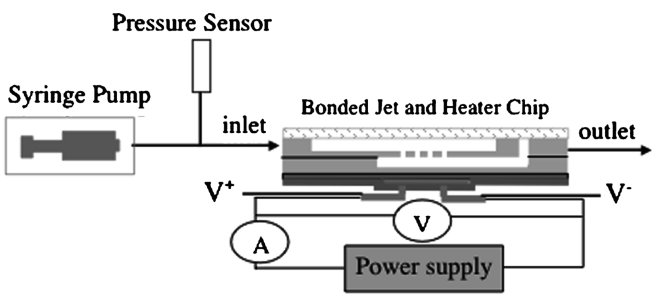

Fig. 5. A schematic of the experimental setup used for microjet characterization. A similar configuration is used for testing with the Intel chip, but a layer of thermal grease is added between the confined jet chip and Intel chip.

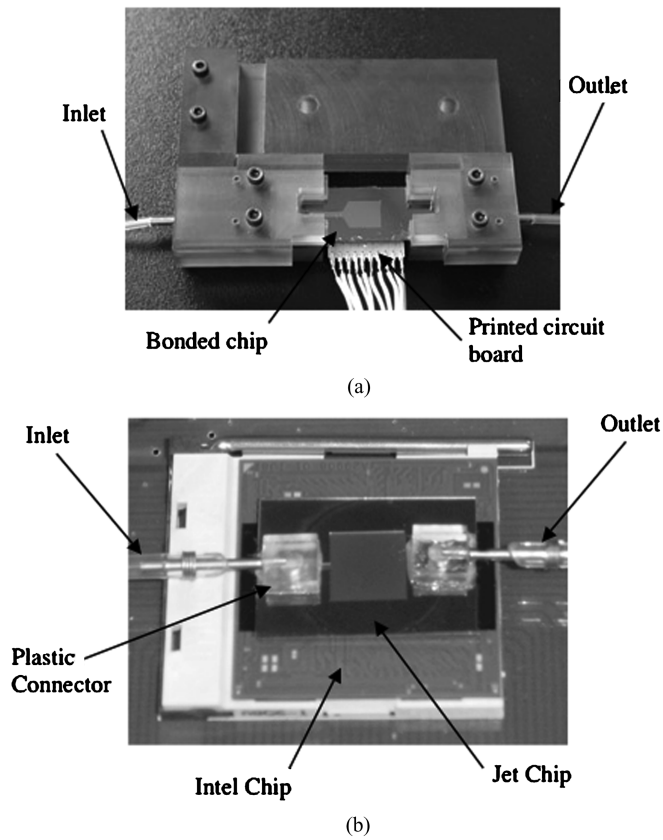

Fig. 6. Pictures of experimental fixturing for confined jet experiments with integrated heater device and Intel chip. (a) Test fixture incorporates fluidic inlet and outlet ports for bonded jet and heater test devices. The jet is on top and the heater is on the bottom with wire-bonded printed circuit boards to make electrical contacts to the thermal sensors. (b) Plastic connectors are glued to top of jet device for the inlet and outlet ports. Thermal grease is sandwiched in between the Intel chip board and jet chip to minimize the interface resistance.

pressure drop between the inlet and the outlet, which is at atmospheric pressure. The pump is first started, and on reaching the necessary pressure for jet formation, power is applied to the heater. This procedure floods the heater reservoir, resulting in submerged impinging jets. The heated fluid is collected from the outlet. All experiments are performed at steady state.

A small printed circuit board is glued to the resistor side of the heater chip device, such that wire bonds for electrical connections can be made from the device through a ribbon cable to a bread board. The resistance values from the heater and thermometers are measured using LabView with a 16-bit 16-channel PCMCIA A/D data acquisition card through a signal conditioning circuit.

The confined jets bonded to the fabricated heater devices are placed into a test fixture, as shown in Fig. 6(a). O-rings in the fixture seal the inlet and outlet ports. The fixture is made from Ultem, which has a thermal conductivity of 0.22 W/mK, to minimize the heat loss due to the fixturing. Fig. 6(b) shows the setup with a confined jet chip placed on top of the Intel test board. The Intel 1 cm^2 thermal test chip dissipates power levels similar to a state-of-the-art microprocessor and is currently used in metal heat sink testing. Plastic connectors are glued on top of the jet chip for the fluidic inlet and outlet ports. Multiple temperature sensors are integrated in the thermal test chip to monitor the junction temperature of the chip. Thermal grease (with a thermal conductivity of 1.1 W/mK) is applied between the chip and the jet heat sink to ensure good thermal contact.

The confined chips are oriented in a horizontal position for simplicity in these experiments. However, gravity is not important in these jet flows, since the jet acceleration is on the order of 10^4 larger than gravitational acceleration. Therefore, the jet chip can be tested in any orientation.

V. Single-Phase Modeling Approach

Single-phase single jets are characterized to aid in understanding jet impingement. The single jet impinges at the center of the chip with an impingement area of approximately $7 \times 10^{-3}\ \mathrm{mm}^2$. The wall temperature profiles at power levels of 4.3 W and 6.7 W using a single 76 μm diameter jet at a flowrate of 2 ml/min are shown in Fig. 7. The temperature profiles are governed by three interacting physical phenomena. The liquid temperature increases with the radial coordinate due to heat received from the wall, and the effective heat transfer coefficient decreases with radial coordinate due to the increasing film thickness. Finally, the symmetry is broken by a net flow of liquid toward the outlet on one side of the heater reservoir, which augments both the liquid temperature and the convection resistance in the vicinity of the outlet. The figure also shows the measured wall temperature profile in the absence of a jet. The decrease in

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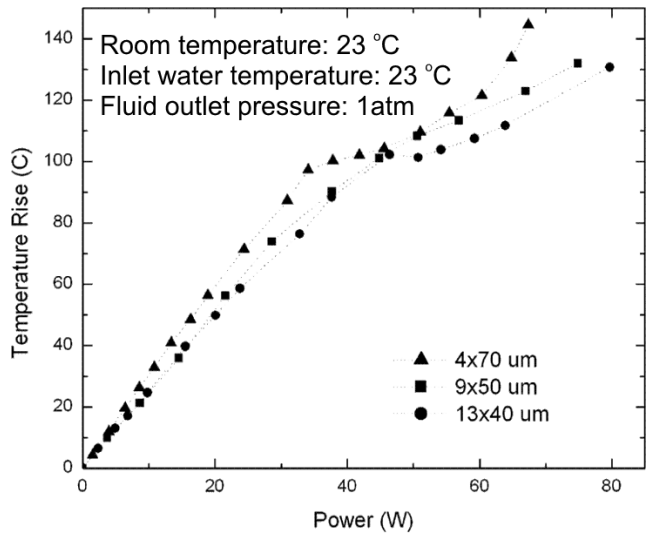

Fig. 7. Experimental and theoretical temperature profiles at varying power levels due to a single 76 μm jet impinging on to the fabricated heater device at a flowrate of 2 ml/min. Temperature of the device in the absence of the jet is also plotted for reference.

temperature on the ends of the device suggests the heat loss associated with the fixturing.

To interpret the data, we develop here a 1-D radial model in cylindrical coordinates, which accounts for conduction in the solid and convection by the liquid. Fig. 8 shows a schematic of the geometry for the model. The model as shown in the schematic assumes that the reservoir is not flooded and the liquid boundary forms from the jet in a reservoir of air. The governing energy equations for the fluid and the solid are

$$\frac{d}{dr}(\rho\delta_f u r i_f) - hr(T_w - T_f) = 0 \tag{1}$$

$$\frac{d}{dr}\left(k_s r \frac{dT_w}{dr}\right) - \frac{hr}{t}(T_w - T_f) - \frac{(T_w - T_\infty)r}{tR''_{\text{env}}} + \frac{q'''r}{t} = 0 \tag{2}$$

where r is the radial coordinate, and t is the thickness of the silicon. The radial model approximates the heated circular area with a radius 0.56 cm, which is equivalent to a square area with a 1-cm length on each side. The heat generation rate per unit volume, q''', is assumed to be uniform throughout the heated region. The average local temperatures of the wall, the fluid, and the environment are $T_w, T_f,$ and T_∞, respectively. The enthalpy per unit mass of the fluid is $i_f = c_p T_f$ where c_p is the specific heat, the silicon thermal conductivity is k_s, the density of the fluid is ρ, the liquid film thickness is δ_f, and the liquid velocity is u. The liquid film thickness is a function of the radial distance r, the Reynolds number Re_d, and the jet diameter d [12]. The thermal resistance per unit surface area, R''_{env}, accounts for heat losses from the chip surface to the surrounding ambient air due to natural convection.

The jet impingement heat transfer coefficient, h, is approximated using macroscale single-phase jet Nusselt number correlations determined by Liu *et al.* [12]. They identified several heat transfer regimes for $\mathrm{Pr} \geq 1$ which include the stagnation zone, the boundary layer region (neither the viscous nor thermal boundary layers reach the free surface), the similarity regions (the viscous boundary layer or/and thermal boundary layer reach the free surface), and the turbulent region. The stagnation Nusselt number was determined by solutions to the boundary layer and energy equations. For the other laminar regions, Liu *et al.* solved the integral energy equation with approximations of the velocity and temperature profile given as

$$u(r,y) = u_m(r)\left[\frac{3}{2}\frac{y}{\delta} - \frac{1}{2}\left(\frac{y}{\delta}\right)^3\right] \tag{3}$$

$$T(r,y) - T_w = (T_f - T_w)\left[\frac{3}{2}\frac{y}{\delta_t} - \frac{1}{2}\left(\frac{y}{\delta_t}\right)^3\right] \tag{4}$$

where u_m is the liquid surface velocity, y is the distance normal to the impingement plane, δ is the viscous boundary layer thickness, δ_t is the thermal boundary layer thickness, T_f is the fluid temperature, and T_w is the wall temperature [12], [26]. The viscous boundary layer thickness, δ, when $\delta < \delta_f$, is approximated as

$$\delta = 2.679\left(\frac{rd}{\mathrm{Re}_d}\right)^{1/2} \tag{5}$$

where r is the radial coordinate, d is the jet diameter, and Re_d is the Reynolds number based on jet diameter. When $\delta \geq \delta_f$, the viscous boundary layer is the same as the liquid film thickness. The thermal boundary layer thickness can be estimated by the conduction thickness

$$\delta_t = \frac{d}{\mathrm{Nu}_d} \tag{6}$$

where d is the jet diameter, and Nu_d is the Nusselt number based on the jet diameter. Nusselt number correlations for the defined regions as a function of Reynolds number, Prandtl number, and jet diameter were determined using this approach. The turbulent heat transfer coefficients downstream were ignored in the analysis since turbulent effects are not present at these length scales owing to the small values of $\mathrm{Re_d}$, which ranges from 600 to 1000 in these experiments. The convection coefficients obtained from the Nusselt number correlations above ranged from 0.072 to 4.4 W/cm^{2}K.

Equations (1) and (2) are discretized using a first-order finite difference approach. The heat removal effect due to the jet impingement is shown on the element with the forced convective term, along with the heat loss due to natural convective losses to the environment. The heat generated per unit volume, q''', from the heater on the chip is depicted on the solid element. The heat removal due to jet impingement of the solid by the liquid is shown by the forced convective term on the fluid element. The discretized equations of all the elements are used to solve for the temperature profile of the heated wall and impinging fluid. An iterative process is used where an initial temperature distribution is assumed along the wall, from which the fluid temperature is calculated. The wall temperature is assumed to have converged when the error is less than 0.1%. The boundary conditions are dictated by the heat loss in the fixturing. This heat loss is estimated by matching the theoretical temperature profile to the

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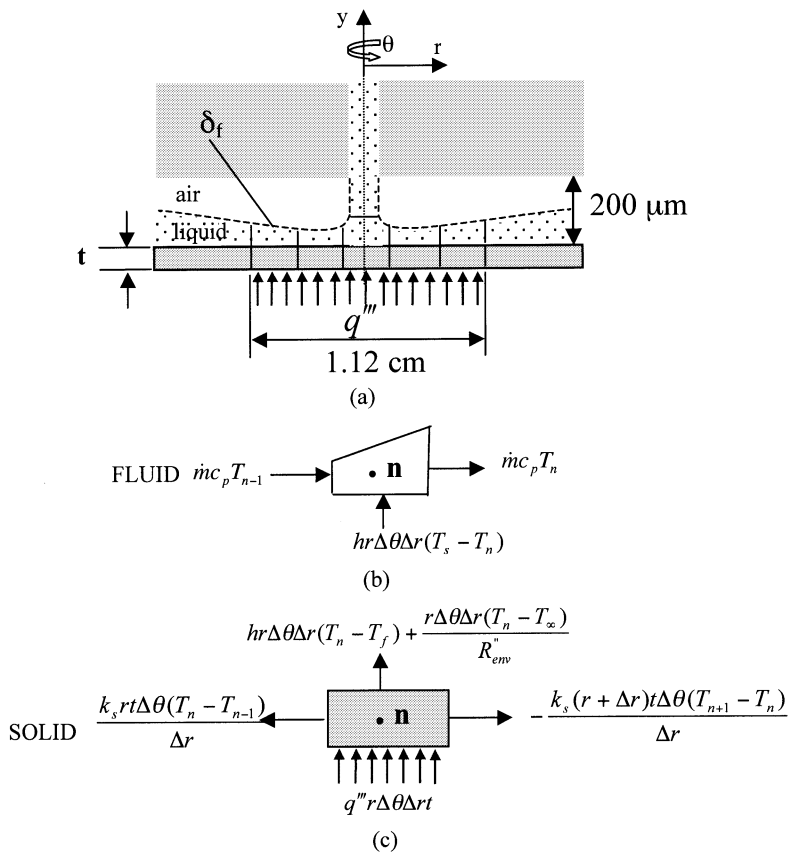

Fig. 8. Schematic of geometry used for radial 1-D conjugate heat transfer analysis of a single jet impinging onto a uniformly heated surface. The variables $r, \theta, h, c_p, T_n, T_f., T_s, \delta_f, \dot{m}, q'''$ are the radial coordinate, the rotation angle about the axis, the heat transfer coefficient of the jet, specific heat of the fluid, the temperature of the nth element, the temperature of the fluid, the temperature of the solid, the liquid film thickness, the mass flowrate, and the heat generation rate per unit volume, respectively. $R''_{\rm env}$ denotes the heat loss from the environment per unit surface area. (a) Schematic of geometry and conditions used. (b) Discretization of the fluid element. (c) Discretization of the solid element.

experimental temperature profile when jet impingement is not present in Fig. 7. The water properties, such as the viscosity and specific heat, and the thermal conductivity of the silicon used in the simulation are those at the average of the wall and inlet fluid temperatures. The dotted lines in Fig. 7 are the modeling results for a single 76 μm diameter jet at power levels of 4.3 W and 6.7 W at a flowrate of 2 ml/min. The simulated temperature profiles show good agreement with the experimental results. The slightly higher temperatures in the predicted results may be a result of the preheating of the water as it enters the top jet reservoir or the conduction losses through the bonded silicon jet chip on top. The model also shows a symmetric temperature profile because it does not account for the presence of the wall which confines the fluid in the lateral direction. Therefore the effect of the net flow of liquid toward the outlet as described above is not shown in the simulation.

VI. Experimental Results and Discussion

The experimental wall temperature profile for a confined single 76 μm diameter jet is compared to that of the array of four 76 μm diameter jets shown in Fig. 9. For each result, the wall temperatures are normalized by the inlet temperature, $T_{\rm wi}$, in order to compare the profiles with differing flowrates and power levels. For reference, temperature sensor readings from the heater device are shown for the case of no jet impingement.

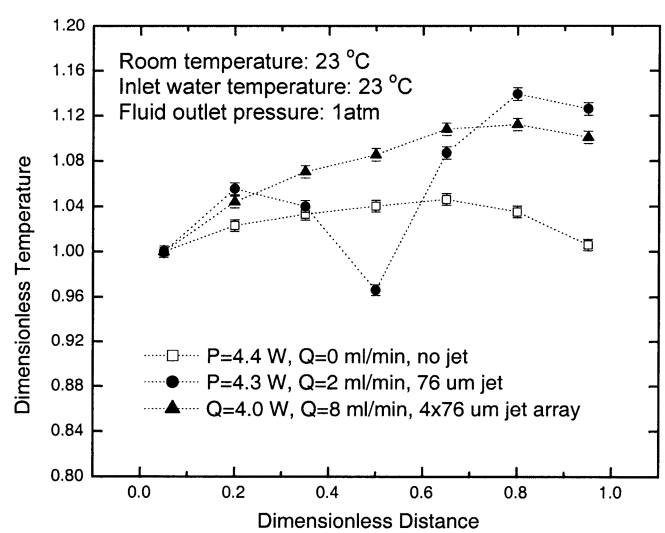

Fig. 9. Comparison of a normalized temperature profile of a single 76 μm jet orifice to a four 76 μm jet array along the heater surface. The distance is normalized by the length of the heated area and the wall temperature is normalized by the inlet wall temperature. This temperature normalization is performed to account for the large difference in flowrates used between the single-jet and four-jet array. The no jet temperature profile is also shown for reference suggesting that there is detectable heat loss at the ends due to the fixturing.

The wall temperature measured at the temperature sensor closest to the inlet for the case of no jet was 99.1 °C, and with

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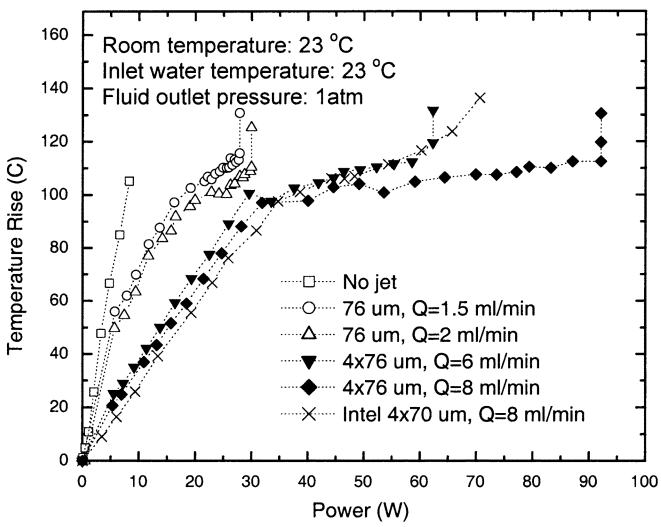

Fig. 10. Comparison of the temperature profiles with increasing power of a single 76 μm jet and a four 76 μm jet array at varying flowrates. The results using the integrated heater devices and the Intel board are also plotted for comparison. The temperature rise is calculated by subtracting the wall temperature when no power is applied from the measured wall temperature. The ambient temperature and water inlet temperature were held constant during the experiments. The uncertainty in these measurements is $\pm 2\%$.

the single-jet and four-jet array were 47.8 °C and 31.8 °C, respectively. The presence of a single jet impinging onto the heater chip causes a local temperature drop of 10% at the point of impingement located 5 mm from the inlet on the heater chip. This demonstrates potential of jet impingement for heat removal of a hotspot where the temperature far exceeds the chip average temperature. The four-jet array demonstrates that a uniform temperature profile can be achieved. The maximum temperature variation using a jet array is within 10% compared to 20% using a single jet. The asymmetry in the temperature profiles, as discussed above, is a result of the net flow toward the outlet from the confined wall.

Fig. 10 shows the relationship between the average wall temperature rise and total power up to levels causing boiling at various flowrates for a single 76 μm diameter jet and a four 76 μm diameter jet array. Using the four 76 μm jet array, removal of 92 W is achieved with a flowrate of 8 ml/min, a pressure drop of 6.9 psi, and temperature rise of approximately 100 °C. The flowrates of the single-jet and multijet array cannot be directly compared due to the necessary different flowrates and pressure drops for jet formation. While the flowrate per jet is the same for both cases, the total flowrate determines the wall temperature and the heat removal capability of the jet heat sink. The flowrate per jet, however, is important in designating the pressure drop required for jet formation. As the flowrate increases, the heat removal rate increases as expected, resulting in a decreased wall temperature.

Similar temperature trends are seen in all cases for the single-jet and four-jet array when power is increased. The initial linear rise in temperature is an effect of single-phase liquid heat transfer with jet impingement and forced convective cooling. The maximum liquid-phase heat transfer coefficient, based on the inlet liquid temperature, is approximately 0.3 W/cm^{2}C.

The second region where the temperature profile is relatively flat is during the fluid phase change from liquid to vapor, utilizing the latent heat of vaporization. The single jet results show a very large temperature rise under two-phase conditions because the single jet is not optimal for cooling an entire 1 cm^2 heated area. The results for the four jets show a lower average temperature corresponding to a boiling convection coefficient, based on the excess wall temperature above saturation, of approximately 3 W/cm^{2}C. The overall heat transfer coefficient, based on the inlet temperature, is approximately 1 W/cm^{2}C. These values are substantially below the theoretical limits available for jet impingement cooling, which suggests that partial flooding of the reservoir may be increasing the level of superheating and causing pool boiling. All of the experiments reached dry-out conditions, specifically with a dramatic increase in temperature, when the quality of the exiting fluid reached approximately 0.3. The quality is defined as the fraction of mass in the vapor phase.

The current levels of superheat from the experiments pose problems in implementation of the cooling system, since acceptable junction temperatures for the VLSI chips are 85 °C as stated by ITRS [1]. However, by incorporating this device in a closed loop, a vacuum pump can be used to decrease the pressure below atmospheric pressure such that the saturation temperature of water can be decreased [27], [28]. With this approach, we anticipate maintaining acceptable junction temperatures with two-phase jets. Furthermore, flowrates and more optimized configurations of the jet arrays and heater device geometry can aid in dissipating more heat from the heated surface as well as minimizing the wall superheat. Future experiments need to visualize the flow regimes and carefully determine the impact of flowrate.

The performance of a four 70 μm jet array on the Intel chip at the same flowrates as the integrated jet and heater devices are also shown in Fig. 10. The sensors on the Intel chip measure the junction temperature of the device, while the sensors on the integrated jet and heater measure the wall temperature. However, due to the high thermal conductivity of silicon and small distance to the chip junction, it is reasonable to assume that the integrated device measures the junction temperature. The average temperature rise as a function of increasing power show good agreement with the performance using the integrated jet and fabricated heater devices during lower temperatures of operation, suggesting that the thermal resistance of the grease is not significant. However, since the jet chip is not clamped down to the Intel chip, the increase in thermal resistance between the jet chip and the Intel thermal test chip, owing to thermal expansion, yielded a substantially higher temperature rise in the two-phase region. Furthermore, since silicon has a high thermal conductivity, the temperature drop from the jet onto the impingement plane spreads laterally. Because the thermal resistance associated with the grease becomes larger than the silicon in the lateral direction with increasing temperature, the cooling effect at the sensor of the Intel thermal test chip is diminished. The combination of the increase in grease resistance and the conduction path in the silicon layers causes this discrepancy in the measurements between the fabricated heater and Intel thermal test board.

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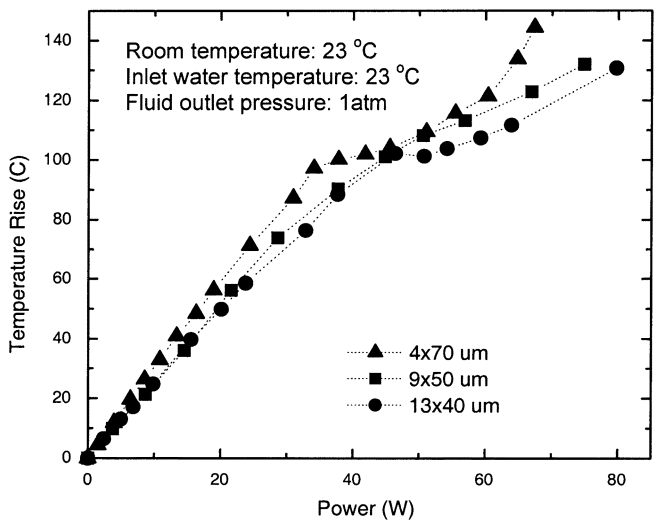

Fig. 11. Comparison of temperature rise as a function of power for different configuration of arrays at the same flowrate of 8 ml/min measured using an integrated temperature sensor Intel thermal test chip along with separate fabricated jets directly impinging onto the chip surface. The ambient temperature and water inlet temperature were held constant during the experiments. The uncertainty in the temperature measurements is approximately $\pm 1\%$.

Three different array configurations are also used to study the removal of heat and temperature profile of an Intel thermal test chip with integrated heater and temperature sensors. A four 70 μm jet array, a nine 50 μm jet array, and a thirteen 40 μm jet array are compared at the same flowrate of 8 ml/min, using the Intel thermal board. The temperature rise measured using an integrated temperature sensor at the center of the chip as the power is increased for the three different array configurations is examined in Fig. 11. As expected, the four 70 μm jet array, causes the highest temperatures at the center of the chip, up to 20 °C higher than the nine 50 μm jet array because a jet orifice is absent, eliminating the stagnation region which provides the most effective cooling. The two other array configurations have stagnation regions at the sensor location, but the thirteen 40 μm jet array achieves the lowest chip junction temperature because it has the highest exiting velocity from the orifice. The jet with the 40 μm orifice accelerates the most due to the largest pressure drop across the orifice. While the flowrate per jet is less due to the increase in the number of jets in the array, the pressure drop governs the jet exit velocity and in the case of the 40 μm jet, the velocity is doubled from the initial velocity. In addition, the smaller orifice size allows a larger number of jets to be placed in the array, which locally reduces the temperature due to the cooling contribution of the surrounding jets. The thirteen 40 μm jet array removes 80 W at a flowrate of 8 ml/min. Tradeoffs exist between the size of the jets, which dictates the number of jets, and the pressure drop. The decrease in size of the jet orifice requires an increase in pressure for a jet to form. The maximum pressure drops in the experiments for the four 70 μm, nine 50 μm, and thirteen 40 μm jet arrays are approximately 7 psi, 10 psi, and 17 psi, respectively. Minimal fluctuations in the pressure are recorded using the three array configurations because the large chamber in the heat transfer region is decoupled from the significant pressure drop which is in the jet orifices.

VII. Conclusion

This paper describes the design and fabrication of single-jet and multijet arrays of diameters ranging from 40 μm to 76 μm. Jet impingement heat transfer is experimentally studied using integrated heater devices and temperature sensors. Predictions from a one-dimensional radial temperature model are in good agreement with the experimental results. The performance of these jets was characterized using fabricated heater devices as well as an industry standard Intel thermal test board. A removal of 90 W has been demonstrated using a four-jet array at a flowrate of 8 ml/min with a 100 °C temperature rise with jet diameters of 76 μm. Boiling heat transfer coefficients of approximately 3 W/cm^{2}C and wall superheat of 30 °C in the experiments suggest the possibility of pool boiling.

The characterization of liquid microjet impingement in this study demonstrates a potential technology for future IC chip cooling. However, reducing the wall superheat and achieving higher heat removal rates requires visualization of the flow regimes and optimization of the flowrates to reduce flooding of the reservoir. A new heater and jet test structure design allowing for optical access is currently underway. Also, quantitative fluorescence imaging methods such as particle image velocimetry (PIV) will be used to examine the flow fields in the confined jet and heater test structures. Furthermore, optimization of the geometry is needed to minimize the large pressure drops in the jet formation process. Alternate geometries, such as square, elliptical, and slot orifices, and optimal orifice lengths and orifice to impingement plane spacings, will be explored to increase heat removal rates.

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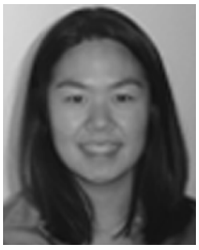

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