

Electrothermal Modeling and Design Strategies for Multibit Phase-Change Memory

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Abstract—Electrothermal transport and crystallization dynamics govern the speed and bit stability of multibit phase-change memory (PCM). This paper develops a transient simulation methodology incorporating electrical, thermal, and phase transition models to investigate multibit PCM cell structures and programming strategies. The simulations evaluate two standard PCM structures, namely, the mushroom cell and the confined pillar cell, with feature sizes smaller than 40 nm. The transient simulation captures the phase distribution and cell resistance profile, which are corroborated by transmission electron microscope imaging and the corresponding measured resistance values. This paper also explores a more compact architecture, i.e., the stacked vertical cell, with precise control of Joule heating and potentially more stable intermediate resistance levels. For an electrode area of $10\text{ nm} \times 20\text{ nm}$, a low programming current of $60\text{--}90\text{ }\mu\text{A}$ generates sufficient heating power to amorphize the phase-change elements sequentially, resulting in four distinct resistance levels distributed over a two-order-of-magnitude resistance range with promise for multibit storage.

Index Terms—Crystalline dynamics, electrothermal simulation, multibit programming, phase-change memory (PCM).

I. INTRODUCTION

PHASE-CHANGE memory (PCM) is a competitive next-generation nonvolatile memory technology due to its high performance, endurance, and scalability [1]. PCM stores information by thermally changing the structural phase of a chalcogenide compound such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST). Multibit operation, in which a single cell stores more than 1 bit of data (e.g., 2 bits/cell requires four resistance levels), can substantially increase PCM data densities. The wide resistivity range between the crystalline and amorphous states, which typically exceeds two to three orders of magnitude, allows sufficient margins for the intermediate resistance levels. Up to 16 resistance levels have been achieved to store 4 bits/cell [2]. However, the resistance drift and programming variation can

blur the separation of the intermediate levels and degrade the reliability of multibit PCM [3], [4]. Although the use of programming algorithms such as write-and-verify can help [2], [5], it significantly compromises the programming speed. Novel phase-change materials [6], [7] and cell architectures [8], [9] can generate more stable intermediate resistances without the write-and-verify sequence. The complex thermal, electrical, and crystallization physics involved in multibit PCM require a fully coupled multiphysics model for effective design and accurate performance predictions.

Past simulation progress on the multibit problem includes establishing an equivalent PCM circuit with a voltage-controlled current source [10], using a lumped thermal resistor to describe the RESET operation [11], and inferring the size of the amorphous GST (a-GST) from measured $I\text{--}\sqrt{V}$ curves [12]. The crystallization process was usually simplified using the Johnson–Mehl–Avrami theory to calculate the crystalline fraction of the GST [13]. However, the resistance of a PCM cell is determined not only by the crystalline fraction but also, more importantly, by the shape and distribution of a-GST, which are not captured by these approximate models. Kim *et al.* proposed an improved simulation method that computed the local crystal fraction to determine the local electrical and thermal conductivity values of the mixed phase [14]. The various existing models and simulation approaches, some of which are still under debate, require careful comparisons and calibrations to the experimental data.

This paper develops a fully coupled electrothermal simulation to predict the temporal evolution of GST phases at very short length and timescales. Section II presents a set of transient thermal, electrical, and phase transition models and compares the computed phase distributions with transmission electron microscope (TEM) images. Section III evaluates the multibit performances of two widely used PCM structures and programming schemes and compares the simulations with existing experimental data. Section IV implements the simulation code to explore a new architecture that yields four distinct resistance levels with improved multibit stability. The results and methodology developed here enable more efficient design of multibit PCM devices.

II. ELECTROTHERMAL MODELING AND ALGORITHMS FOR PHASE EVOLUTION

PCM involves a rich set of coupled electrical, thermal, and phase-change phenomena. For a volume of a-GST subject to a voltage less than the threshold voltage V_{th} , the current

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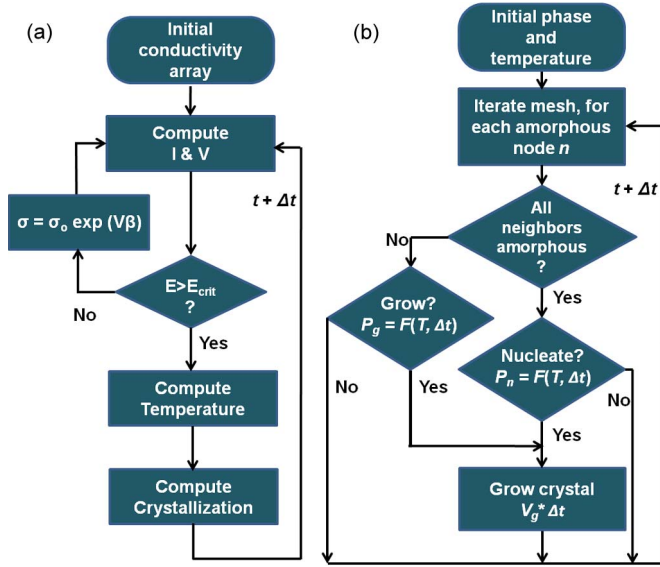


Fig. 1. Key computational flows implemented in the coupled simulation. (a) The electrical model compares the local electrical field with the critical field before solving for the temperature and phase. (b) The GST crystallization algorithm considers two parallel mechanisms, i.e., probabilistic nucleus formation and crystalline growth, both as functions of cell temperature T and time duration Δt .

exponentially grows and can be described by the Poole–Frenkel model [15] as

$$I = I_{\text{PF}} e^{\beta_{\text{PF}} V_A^{1/2}} \quad (1)$$

where V_A is the applied voltage, and I_{PF} and β_{PF} are material constants. The simulation code numerically evaluates the local electrical field and current density by applying (1) to each mesh grid in the a-GST volume. The algorithm shown in Fig. 1(a) compares the local electric field E to the critical value E_{crit} and adjusts the electrical conductivity accordingly. Threshold switching happens when the local electric field exceeds the critical value. The local temperature and phase are subsequently determined after switching. Since the electric field nonuniformly distributes in a PCM cell depending on its geometry and amorphous level, this paper iteratively finds the field-dependent electrical conductivity σ at each node using $\sigma = \sigma_0 \exp(V/\beta_{\text{PF}})$, where V is the local voltage.

The thermal model for a PCM cell involves 3-D anisotropic heat conduction as described using

$$\frac{1}{D_i} \frac{\partial T_i}{\partial t} = \eta_i \left(\frac{\partial^2 T_i}{\partial x^2} + \frac{\partial^2 T_i}{\partial y^2} \right) + \frac{\partial^2 T_i}{\partial z^2} \quad (2)$$

where D_i is the thermal diffusivity of layer i , and $\eta_i = k_{xy}/k_z$ captures the anisotropy ratio between the in- and cross-plane thermal conductivity values [16]. The nonhomogeneity and defects in the material, which were neglected in (2), can lead to filament growth of conduction paths, which may alter the temperature distribution. The thermal boundary resistance (TBR) at the material interfaces dominates the nanometer-scale thermal conduction problem and can strongly influence the temperature response of the cell [17]. For this reason, we add the TBR to the interlayer boundary condition using

$$\vec{q}_i'' = (T_j - T_i)/R_b \quad (3)$$

where $\vec{q}_i''$ is the heat flux normal to the interface, R_b is the TBR, and T_i and T_j are the temperatures of the adjacent layers. The TBR also shifts the location of the amorphous region toward the heater interface due to the enhanced thermal resistance, an effect to be discussed in the following section.

We use a probabilistic crystallization and nucleation model to evaluate the phase-change transition in the PCM cells [18]

$$P_n = \alpha \Delta t \exp \left\{ -\beta \left[E_a + \frac{A}{(\Delta G)^2} \right] \right\} \quad (4)$$

where P_n is the probability of an amorphous small volume to become a crystalline nucleus during time interval Δt . E_a is the activation energy associated with the nucleation, ΔG is the excess Gibbs free energy of the amorphous phase, and A is determined by the interfacial surface free energy at the phase interface. Frequency factor α relates to the atomic vibration, and parameter β is defined as $1/k_B T$, where k_B is Boltzmann's constant. Alternatively, a small volume may become crystalline due to the growth of an adjacent nucleus. Crystalline growth velocity V_g can be written as [18]

$$V_g = f a_0 \alpha [1 - \exp(-\beta \Delta G)] \exp(-\beta E_{a2}) \quad (5)$$

where f is a parameter that relates to the temperature and crystalline growth mode, a_0 is the atomic jump distance, and E_{a2} is the activation energy associated with atomic diffusion. The model applies these two mechanisms in parallel, as shown in Fig. 1(b), to determine the phase distribution.

This paper uses a “mushroom” vertical cell geometry similar to those developed in [2] to implement the coupled electrothermal-phase transition models. Commercial software COMSOL defines the geometry and material properties, and it computes the temperature fields for each time step. A set of MATLAB codes implements the electrical switching and phase-change algorithms. The symmetry of the device geometry reduces computation time by using only a quarter cell, as illustrated in the inset in Fig. 2(a). In this demonstrative simulation, the top electrode contact (TEC) and the bottom electrode contact (BEC) are made of tungsten. A TiN heater delivers heating power while reducing atomic interdiffusion with the phase-change chalcogenide. The phase transition occurs in a region very close to the interface between GST and the heater. The TBR at this interface helps enhance the thermal insulation from the cold metal components and reduces the required programming power. The simulation uses thermal conductivity values of 0.56 W/mK for crystalline GST (c-GST) and 0.18 W/mK for a-GST at room temperature [16]. The temperature dependence of thermal conductivity up to 350 °C has been measured in previous studies [19], [20], and this simulation assumes constant conductivity beyond 350 °C because the short timescale inhibits further transition to the hexagonal close-packed phase. The heat capacity of GST is $C = 1.3 \times 10^6$ J/m³K and assumed constant for different temperatures and phases [14], [21]. Future measurement on the temperature-dependent C above melting point can further improve the accuracy of this simulation because it may affect the thermal time constant of the PCM cell. The TBR between GST and the surrounding material is estimated at 20 m²K/GW based on

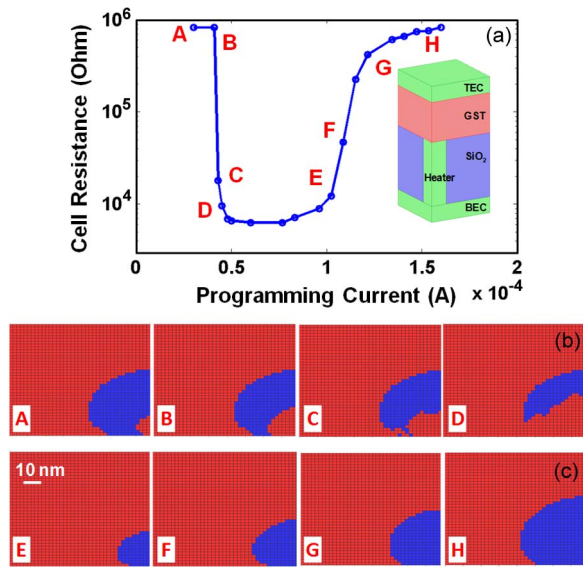


Fig. 2. Simulation results of phase transitions in a mushroom-shaped PCM device. (a) Simulated $R-I$ characteristics of a PCM cell. SET operation occurs in A–D, whereas E–H correspond the RESET process. (Inset) Schematic of the PCM cell. (b) Cross-sectional view of the GST phase distribution after a SET operation with different current amplitudes. (c) GST phase distribution after a RESET process with varying current amplitudes. Red and blue colors represent crystalline and amorphous phases, respectively.

previous measurements [22] and is assumed to be temperature independent.

An electrical current pulse induces the SET process causing the cell to transit from a high-resistance state into a low-resistance state, as shown from A to D in Fig. 2(a). The phase transition involves electrical switching in addition to the thermal effects. Equation (1) suggests that the electrical conductivity of the amorphous region exponentially increases with the voltage before threshold switching. This increase in conductivity causes an even larger current to flow through the amorphous region until the critical electric field is reached for threshold switching, which, in this case, is approximately 1 MV/cm [15]. Following threshold switching, the significantly larger current flowing through the device raises temperature in the amorphous volume, which is sufficient for crystallization. Fig. 2(b) shows the different levels of crystallization of the original a-GST region after SET pulses with varying amplitudes. For an ideally homogeneous GST layer free of defects as assumed in this simulation, the crystallization process starts from the location close to the heater electrode and grows outward owing to the higher temperature in that region.

A RESET current pulse with larger amplitude and shorter pulsewidth melts and subsequently quenches the GST active region into the amorphous state. We use an electric pulsewidth of 10 ns and rise/fall time of 3 ns/3 ns, respectively. The initial cell is in the crystalline phase with a low electrical resistance before the pulse. Intense Joule heating from a RESET current pulse causes the region close to the heater electrode to melt and quench subsequently. This forms a dome-shaped amorphous region near the heater, the volume of which increases with increasing current amplitude, as shown in Fig. 2(c). The high electrical resistance state can be achieved with sufficiently large amplitude, as shown in the $R-I$ characteristic curve in

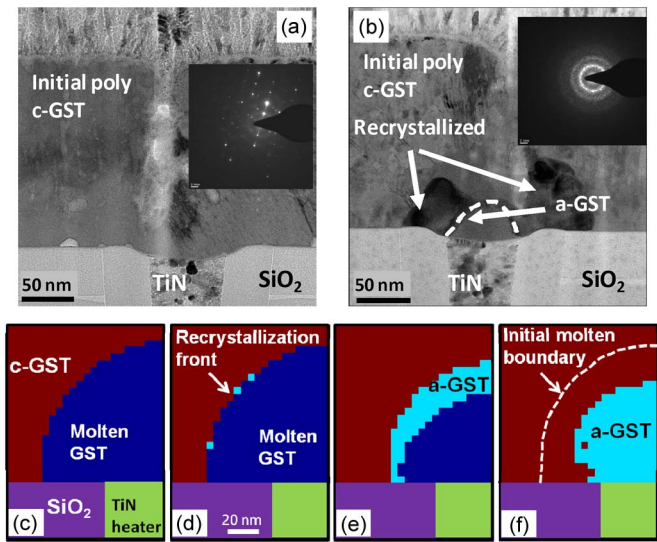


Fig. 3. Comparison of TEM images and the simulated phase distribution after RESET pulses. Cross-sectional TEM images are taken with a similar device [33]. (a) The GST film is polycrystalline (c-GST) in the initial SET state as confirmed by the electron diffraction pattern in the inset. (b) The a-GST cap is formed on top of the TiN heater after RESET operation. (Inset) Electron diffraction pattern corresponding to the a-GST cap region. (c)–(f) Simulated transient phase distribution during a partial RESET process.

Fig. 2(a). The sharp slope between E and G leads to fast switching between the low- and high-resistance states. However, it also introduces difficulties in controlling the intermediate states, which will be discussed in the next section.

In order to verify and calibrate the models developed here, we compare the simulated phase distribution after a partial RESET operation to the TEM images. Past work [23] identified the phase distribution of a vertical PCM cell at SET and partial RESET states. Electron scattering pattern confirms the polycrystalline phase in the initial SET state, as shown in Fig. 3(a), and a partial RESET operation forms an amorphous cap on top of the heater, as shown in Fig. 3(b). Abnormally large grains of c-GST are found around the amorphous cap with substantially different textures from the initial c-GST region. Several other studies also observed similar phenomenon after a RESET pulse and inferred the possible shrinkage of amorphous region after RESET pulse [12], [24]. Our transient simulation captures this effect reasonably well and reveals the detailed phase transition dynamics. First, the active region in the GST layer melted during a RESET pulse [see Fig. 3(c)]. As the cell starts to cool, several nodes at the liquid–solid interface start to nucleate or solidify into a-GST [see Fig. 3(d)], the probabilities of which depend on the temperature and the cooling rate, as discussed earlier in this section. Nucleation and crystal growth inside the amorphous region are also possible if the temperature remains between the crystallization temperature and the melting point during time interval Δt . The competition between the recrystallization and quench-amorphization processes determines the shape and volume of the final amorphous cap, which is always smaller than the initially molten volume, as shown in Fig. 3(f). The recrystallized region undergoes rapid phase change, resulting in different grain sizes around the final amorphous cap than the initially annealed c-GST as observed in the TEM images.

The SET process involves electrical transport before switching and a phase-change process after switching. The theoretical model with an ideal homogeneous material quality predicts that the current flows through the entire amorphous volume. However, the current can also trickle through filament-shaped conduction paths that have the least resistance in the amorphous state [25]. Due to the nonequilibrium distribution of electrons in traps from the equilibrium states (e.g., Fermi level) developed at high fields [15], switching happens and a large current flows through these filaments. Subsequently, the crystallization process initiates around this filament and eventually crystallizes the entire amorphous region. Kuzum *et al.* [26] reported experimental evidence of the polycrystalline filaments embedded in the amorphous regions after a partial SET process. However, the present simulation model assumes a more homogenous current flow during the SET process, which generates an over-idealistic phase distribution, as shown in Fig. 2(b). The strong electric field near a crystalline filament facilitates the nucleation of additional conductive particles at the end of the filament, making it longer and resulting even larger local electric field [27]. As a result, the required voltage to set a cell based on the filamentlike crystallization mechanism may be lower than predicted by the simulation. The future versions of this simulation will incorporate the filament-based conduction model for the SET process.

III. MULTIBIT PCM PERFORMANCE ANALYSIS

The vertical mushroom cells similar to that in the inset in Fig. 2(a) have been explored for multibit programming [2], [28]. Varying the amplitude of the programming pulse can control the cell resistance by delivering different amounts of heating power, which forms the amorphous cap on top of the heater. However, the sharp transition between the low- and high-resistance states, as shown in Fig. 2(a), makes it difficult to precisely control the intermediate resistances. Here, we investigate another strategy proposed in [2], in which the tail duration of a current pulse determines the resistance level by adjusting the cooling rate of the cell. Atoms in the molten phase can be frozen into a disordered amorphous structure if the cooling rate is faster than the crystallization rate. The crystalline growth of GST requires a proper temperature range and a sufficient period of time during which the temperature stays in this range. The thermal time constant scales with the cell resistance and heat capacity. The former is determined by the heater contact area and the resistivity of the GST layer, whereas the latter mostly scales with the volume of the PCM cell. The transient simulation of the vertical cell shows a thermal time constant of ~ 5 ns, which is of the same order of magnitude as the nucleation time. Therefore, a RESET pulse tail duration period much longer than the thermal time constant can facilitate the recrystallization process, which leads to a lower cell resistance.

Fig. 4 demonstrates the control of intermediate resistances by changing the tail duration t_{fall} of a RESET pulse. In this simulation, a rise time t_r of 5 ns induces fast heating, and the active region of GST is melted during the pulsewidth t_w of 25 ns. As the current amplitude decreases and the temperature drops, the molten GST can either nucleate and grow to the

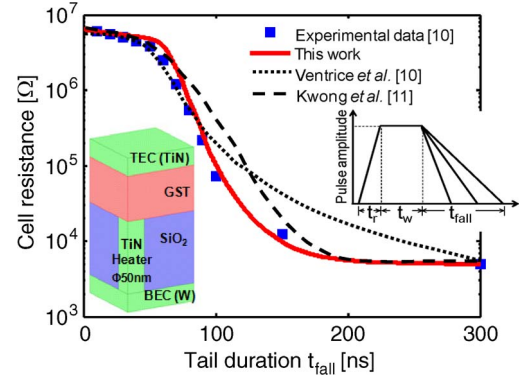


Fig. 4. Mushroom cell resistance as a function of the tail duration of a RESET current pulse. Experimental data are taken from [10]. This work achieves improved prediction of the transitional behavior of the cell resistance. (Inset) Mushroom cell schematic used in this simulation and the shape of a RESET pulse.

TABLE I
ELECTRICAL CONDUCTIVITY σ , THERMAL CONDUCTIVITY k , AND HEAT CAPACITY C OF THE ELECTRODE AND INSULATOR MATERIALS USED IN THE SIMULATION

	σ [S/m]	k [W/mK]	C [J/m ³ K]
TiN	1×10^6 ^a	15 ^b	3.2×10^6 ^a
W	7.1×10^6 ^c	175 ^a	2.58×10^6 ^a
Cu	5.4×10^7 ^d	356 ^d	3.4×10^6 ^c
SiO2	1×10^{-14} ^a	1.2 ^f	3.1×10^6 ^a

^a Ref. [14], ^b Ref. [29], ^c Ref. [30], ^d Ref. [31], ^e Ref. [32], ^f Ref. [33]

crystalline phase or quench to the amorphous phase, depending on the temperature and cooling rate [see Fig. 3(c)–(f)]. The final shape and volume of the amorphous region determine the cell resistance. Tail duration periods from 20 to 200 ns successfully control the intermediate resistances between SET and RESET levels. In order to test and verify the accuracy, we compare the simulation results from this work with experimental data from [10]. The simulated resistance can be affected by the systematic error in the computational algorithm and the uncertainties in the input material properties. We calibrate the high- and low-resistance bounds to the experimental data to facilitate comparison and to reduce the impact of systematic offset. Since detailed material properties are not available in [10], we use the GST properties in Section II and the electrode material properties shown in Table I. The model from this work predicts the resistance change as a function of the tail duration, which achieves good agreement with experimental data. Fig. 4 also compares the model from this work with those reported previously. The general trend of the resistance change can be captured by all three models. However, the ones in [10] and [11] result in relatively large deviations in the intermediate resistances, which are important to the multibit PCM applications. This difference most likely results from the fact that these models are based on the GST crystalline fractions without considering the shape of the amorphous cap. By computing the detailed phase distribution, this work improves the accuracy in predicting the resistance transition behavior of a PCM cell.

Another widely used PCM structure features a confined GST element between the heater and the electrode [34], as

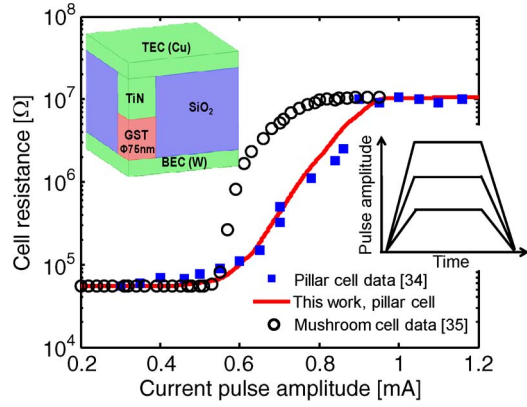


Fig. 5. Amplitude-controlled cell resistance after a RESET current pulse. Experimental data of the confined pillar cell are taken from [34]. The simulated intermediate resistances match reasonably well with measured resistance evolution. The pillar cell yields more gradual resistance change compared with a mushroom cell controlled by the same amplitude-based scheme [35]. (Inset) Confined pillar cell schematic and the shape of RESET pulses with varying amplitudes.

illustrated in the inset in Fig. 5. In this simulation, the diameter and height of the confined GST element are 75 and 50 nm, respectively, which represents the current fabrication technology [34]. The confined pillar structure improves the heating efficiency because it generates Joule heating in the center of the GST element and away from the GST–electrode interface. The TBRs around the GST element further impede the heat loss through the surrounding electrodes and dielectrics. The RESET pulses with varying amplitudes induce different levels of amorphization in the GST pillar, leading to a resistance profile, as shown in Fig. 5. The RESET programming pulse in this simulation features rapid rise time and tail duration of 5 ns each and a pulsewidth of 65 ns. The near-logarithmic relationship between cell resistance and pulse amplitude from 0.6 to 0.9 mA is consistent with experimental data [34]. As a comparison, we overlay in Fig. 5 the results from an amplitude-controlled mushroom cell [35] that has a similar transition current of 0.55 mA. We normalize the resistance data from the mushroom cell to the upper and lower bounds of the pillar cell while preserving the values of pulse amplitude in order to compare their transitional behaviors. The pillar cell structure yields a more gradual R – I curve than the mushroom cells for the same transition current amplitude, indicating more effective control of the intermediate resistance states. As shown earlier, the resistance of a mushroom cell is predominantly determined by the phases near the GST–heater interface. Instead of forming an amorphous cap that abruptly blocks the heater contact area as in the mushroom cell (see Fig. 3), amorphization occurs gradually from the center of the confined GST element in the pillar cell, which offers a more gradual resistance change as a function of current pulse amplitude.

IV. NOVEL CELL GEOMETRY AND MULTIBIT DESIGN STRATEGY

One of the biggest challenges for multibit PCM is the poorly separated resistance levels owing to the continuous transitions of R – I characteristics, a problem that is augmented by the

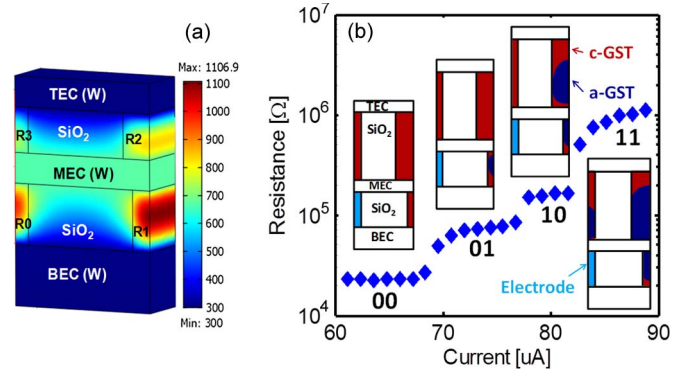


Fig. 6. Stacked vertical multibit cell. (a) Schematic and representative temperature distribution of the cell. (b) Simulation results of the multibit programming with four distinct resistance levels. (Insets) Phase distributions at each of the four resistance levels. Red, dark blue, and light blue colors denote c-GST, a-GST, and tungsten electrodes, respectively.

drift of resistance in the amorphous condition [5], [36]. The write-and-verify technique can mitigate this problem, but it introduces substantial overhead in programming latency [2], [5]. The uncertainty in cell resistance can be significantly reduced if the R – I characteristics exhibit distinct staircase resistance levels over a certain range of programming currents. Past research has explored several implementations, including stacking chalcogenide layers with different stoichiometries and resistivities [6], [7], [37] and novel PCM architectures that rely on the asymmetric temperature distribution in the cell [8], [9]. These implementations generally occupy large areas owing to their lateral or parallel structures.

Here, we explore the potential of a stacked vertical multibit cell, which achieves four distinct resistance levels in a much reduced device footprint. The model developed in this paper provides a valuable tool to accurately predict the phase distribution and analyze the performance of the novel cell structure. Fig. 6(a) shows the cell structure. Two heating elements are connected in parallel on each of the two floors. The confined GST elements with thickness less than 10 nm can be fabricated by the sidewall deposition technique that has been extensively developed [8], [38]. The BEC, TEC, and the middle electrode contact (MEC) are made of tungsten, which is a good thermal and electrical conductor, in this demonstrative design. Potential optimizations include using TiN as an electrode material to minimize diffusion between GST and the electrode. The MEC is floating electrically and thermally, decoupling the heating power of the GST elements on the two floors. The heating power for R_1 , for instance, can be written as $P_1 = I^2 R_1 / (1 + R_1/R_2)^2$, where I is the applied programming current, and R_1 and R_2 are the electrical resistances of the two elements on the lower floor. A representative temperature map of the cross section of the device is shown in Fig. 6(a) where the temperature of each GST element is clearly separated, leading to effective control of the phase change in each GST element. Four resistance levels can be achieved by controlling the states of the three GST elements, as shown in the insets in Fig. 6(b). The width of each GST element determines its current density, temperature, and the resulting phase distribution. In this design, the widths of the four heating elements R_0 – R_3 are 10,

10, 30, and 10 nm, respectively, and the depth of the device is 20 nm. The heights of the elements are 60 nm for R_0 and R_1 and 120 nm for R_2 and R_3 . The three GST elements amorphize sequentially after RESET pulses with amplitudes from 60 to 90 μA and a pulsewidth of 65 ns, yielding a two-order-of-magnitude resistance margin. The small contact area of the GST elements enables an order-of-magnitude reduction in programming current compared with other designs [2], [8], [34]. A SET current pulse with amplitude of 35 μA and duration of 200 ns crystallizes all the GST elements and sets the cell to low-resistance level.

V. SUMMARY AND CONCLUDING REMARKS

Multibit operation is an important enabling feature that can allow PCM to compete with other nonvolatile memory technologies. The electrothermal simulations developed here have revealed that the thermally induced transient phase transitions are critical to multibit programming. Recrystallization from the melted phase during a RESET operation reduces the volume of a-GST as a function of the thermal time constant of the PCM cell. The coupled electrothermal modeling improves the accuracy in predicting the intermediate phase distributions and cell resistances, both of which are important in multibit PCM operations. The inefficient intermediate resistance control limits the multibit capability of the standard cell structures such as the mushroom cell and the confined pillar cell. In this paper, we have explored the operation of a stacked vertical cell structure, which allows the programming current to be reduced by an order of magnitude compared with conventional PCM cells.

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