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Enhanced Thermal Conduction Through Nanostructured Interfaces

Woosung Park¹, Aditya Sood^{a,b}, Joonsuk Park^b, Mehdi Asheghi^a, Robert Sinclair^b, and Kenneth E. Goodson^a

^aDepartment of Mechanical Engineering, Stanford University, Stanford, California, USA; ^bDepartment of Materials Science and Engineering, Stanford University, Stanford, California, USA

ABSTRACT

Interfaces dominate heat conduction in nanostructured systems, and much work has focused on methods to enhance interfacial conduction. These approaches generally address planar interfaces, where the heat flux vector is everywhere normal to the interface. Here, we explore a nanostructured interface geometry that uses nonplanar features to enhance the effective interfacial conductance beyond what is possible with planar interfaces. This interface consists of interdigitating Al pillars embedded within SiO₂ with characteristic feature size ranging from 100 to 800 nm. The total sidewall surface area is modulated to highlight the impact of this additional channel by changing the pillar-to-pillar pitch L_p between 1.6 μm and 200 nm while maintaining the same Al:SiO₂ fill fraction. Using optical pump-probe thermoreflectance measurements, we show that the effective conductance of an ~ 65 nm thick fin layer monotonically increases with decreasing L_p and that the conductance for $L_p = 200$ nm is more than twice the prediction for a layered stack with the same volume ratio and a planar interface. Through a combination of Boltzmann transport modeling and finite element calculations, we explore the impact of the pitch L_p and the pillar aspect ratio on effective thermal conductance. This analysis suggests that the concept of nanostructured interfaces can be extended to interfaces between diffusive and quasi-ballistic media in highly scaled devices. Our work proposes that the controlled texturing of interfaces can facilitate interfacial conduction beyond the planar interface regime, opening new avenues for thermal management at the nanoscale.

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KEYWORDS

interfacial thermal conduction; time-domain thermoreflectance; thermal boundary resistance; nanostructured interface

Introduction

Interfaces strongly influence thermal transport in nanostructured systems and have become a primary impediment to thermal management in many applications such as nanoelectronics [1, 2], energy conversion devices [3–5], and nanophotonics [6–8]. Much research has targeted an improved understanding of the impact on the thermal interfacial resistance of the phonon density-of-states mismatch [9, 10], near-interfacial defects such as vacancies and dislocations [11–15], interface roughness [16–18], phonon inelastic scattering [19–21], electron–phonon interactions [22–25], among other factors. Current approaches to enhancing interfacial thermal transport rely primarily on improving interface quality, accomplished by reducing surface roughness and mitigating near-interfacial defects [21, 26, 27] or through the introduction of vibrational and lattice-matching interlayers [17, 28]. While the specifics vary, the unifying theme among existing approaches is that they involve planar interfaces, where the heat flux vector is everywhere parallel to the surface normal. In order to push the limits with planar interfaces, new approaches are required that can enhance thermal transport beyond what is currently possible.

CONTACT Kenneth E. Goodson  goodson@stanford.edu  Department of Mechanical Engineering, Stanford University, 440 Escondido Mall, Stanford, CA 94305, USA.

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Nomenclature

C	heat capacity
d_{grain}	grain size
L_C	healing length along the layer of the nanostructured array
L_P	pillar-to-pillar pitch
R''	volumetric thermal resistance
s	band/mode index
TBR''	thermal boundary resistance
t_{Pillar}	thickness of pillar
V_{in}	in-phase voltage signal on lock-in amplifier
V_{out}	out-of-phase voltage signal on lock-in amplifier
v	velocity of energy carriers
w_{Pillar}	width of Al pillar

Greek symbols

κ	thermal conductivity
κ_{Al}	thermal conductivity of an Al transducer, $\sim 94 \text{ W m}^{-1} \text{ K}^{-1}$
κ_{NFA}	thermal conductivity of a nanostructured fin array in cross-plane direction
κ_{Pillar}	thermal conductivity of an Al pillar
κ_{SiO_2}	thermal conductivity of SiO_2 , $1.38 \text{ W m}^{-1} \text{ K}^{-1}$
Λ	mean free path of energy carriers
ω	angular frequency of a phonon

Subscripts

boundary	due to boundary scattering
bulk	due to scattering mechanisms in bulk Al
SW	sidewall interfaces

In this work, we explore an interface geometry that includes nonplanar features with characteristic length scales down to 100 nm. Through the creation of nanofabricated fin-like projections, we increase the total area of contact and make the interfacial heat flow three-dimensional in localized regions. This nonplanarity increases the area for heat flow, which enhances the effective interfacial conductance. Our approach is inspired by macroscale fin arrays that are conventionally used to enhance heat transfer between solid surfaces and fluids by increasing contact area [29]. Previous research has explored the use of microstructured surfaces for thermal interface materials at the chip packaging level [30, 31], and computational studies have suggested that the extension of this idea to atomic length scales can be beneficial to interfacial conduction [32]. However, the demonstration of nanostructured interfaces between solids in intimate contact—for example, a stack of layered thin films—has proved challenging so far. Here, we demonstrate that a significant enhancement in thermal conduction is possible in a nanoscale solid-state fin array when the fin-pitch becomes comparable to the thermal healing length along the layer of nanostructured interfaces [33]. Using Boltzmann transport modeling and finite element simulations, we show that the thermal conduction across sidewall interfaces plays an increasingly important role in the conduction across structured interfaces as fin dimensions decrease. We propose that controlled nonplanarity can be useful for enhancing the effective thermal conductance of an interface between any pair of solid materials with sufficient contrast in thermal conductivity and comparable magnitudes of volumetric and interfacial resistances.

Thermal characterization of nanostructured fin array

We explore the concept of nanostructured interfaces experimentally by fabricating a nanostructured fin array (NFA) between adjacent layers of Al and SiO₂. The fin array includes a layer of interdigitating teeth-like structures extending between Al and SiO₂, with cuboidal pillars of Al embedded within the SiO₂ in the form of a periodic square lattice, as shown in Figure 1. The pillars have a nominal thickness of ~65 nm and a constant Al:SiO₂ fill fraction of 1:3. The square lattice has a pitch L_P that varies between 200 nm and 1.6 μm . With decreasing L_P (while maintaining constant thickness), the aspect ratio of Al pillars increases, which leads to increased contact area at the sidewall interfaces. Direct contact between the Al pillars and the top contiguous Al layer used for thermoreflectance measurements ensures that this configuration effectively acts to extend the area of contact between adjacent layers of Al and SiO₂ through the creation of finger-like extensions at the interface (see Supplementary Information for sample fabrication details). At constant fill fraction, as L_P decreases, a larger fraction of the heat flux from the Al to SiO₂ flows through the Al pillars, causing an increase in the effective conductance of the structured interface. We compare the effective thermal conductivity of the nanostructured fin layer with that of the reference stack, which is defined as a layered structure with the same Al:SiO₂ volume ratio and Al-SiO₂ thermal interfacial resistance with no nanostructured fins present.

Time-Domain thermoreflectance

We measure the effective thermal conductivity of the nanostructured fin array layer in the film-normal direction, κ_{NFA} , using time-domain thermoreflectance (TDTR), an optical pump-probe technique [11, 34, 35]. TDTR technique utilizes ~9 ps optical pulses from a pump source to heat up the surface of a sample coated with a thin Al transducer layer and time-delayed probe pulses to interrogate the temporal changes in transducer reflectivity as heat diffuses into the sample of interest (see Supplementary Information for the details of TDTR). A schematic of our multilayer sample stack is shown in Figure 2a. We treat the stack as including three layers on top of a semi-infinite silicon substrate: (from top to bottom) the Al transducer, the nanostructured fin array layer, and SiO₂. The fin array layer is assumed to be laterally homogeneous and isotropic, although we are insensitive to its in-plane conductivity because the thermal penetration depth (~250 nm at 4 MHz) is

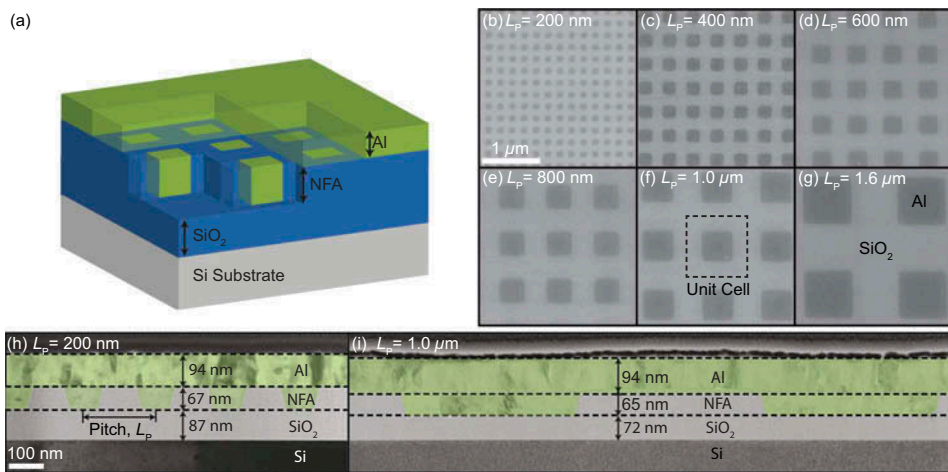


Figure 1. (a) Schematic of an NFA. (b)–(g) Plan-view scanning electron microscopy images for samples with different pitches L_P , taken before deposition of an Al transducer layer. (h), (i) Cross-sectional transmission electron microscopy images for samples with $L_P = 200$ nm and $L_P = 1.0$ μm . The Al regions in the nanostructured fin array and the top transducer layers are false-colored in green. (b)–(g) and (h)–(i) share scale bars shown on (b) and (h), respectively.

much smaller than the laser spot size ($\sim 10 \mu\text{m}$). We assume literature values for the thermal conductivity of the SiO_2 and Si [36] and for the volumetric specific heat of the Al [37], SiO_2 [38], and Si [39]. To determine the thermal conductivity of the Al transducer layer, we perform four probe measurements of electrical conductivity of a patterned metal line on an SiO_2/Si substrate, which is metallized at the same time as the transducer layers for TDTR samples. Using the Wiedemann-Franz law, the thermal conductivity of the transducer layer is estimated to be $\sim 94 \text{ W m}^{-1} \text{ K}^{-1}$. Because all of the samples are prepared on the same wafer, we assume that they have the same Al transducer conductivity. The thermal interfacial resistance between the Al transducer layer and SiO_2 is measured using TDTR and is found to be $\sim 4.4 \text{ m}^2 \text{ K GW}^{-1}$ on a sample composed of Al (94 nm)/ SiO_2 (157 nm)/Si. We assume that this thermal interfacial resistance also applies between the Al transducer and the nanostructured fin array layer in all of our samples. The thermal interfacial resistance between SiO_2 and Si is assumed to have a nominal value of $5 \text{ m}^2 \text{ K GW}^{-1}$ [40]. The volumetric specific heat of the fin layer is taken to be a 1:3 volume-weighted average of Al and SiO_2 . This leaves the cross-plane thermal conductivity of the fin layer, κ_{NFA} , as the only unknown parameter, which is extracted by fitting the data to the 3D heat diffusion model. In a later section, we calculate the performance of hypothetical, highly scaled fin arrays where quasiballistic effects within the Al might become more important. Error bars in κ_{NFA} are predominantly based on uncertainties in the

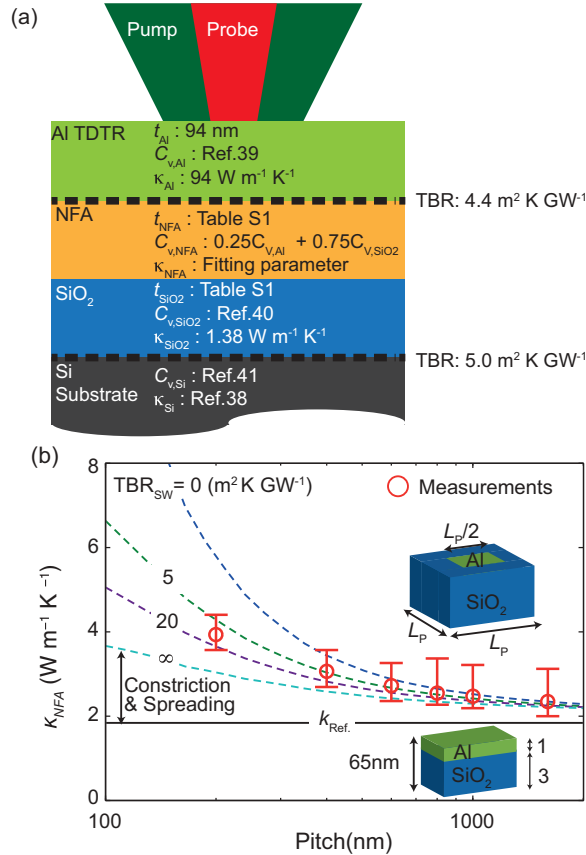


Figure 2. (a) Schematic of sample stack used to analyze time-domain thermoreflectance data. The NFA is assumed to be a homogeneous layer. t , C_v , and κ denote thickness, volumetric heat capacity, and thermal conductivity of a layer, respectively. Dashed lines indicate interfaces with finite resistance. (b) Effective cross-plane thermal conductivity of the nanostructured fin array layer, κ_{NFA} , as a function of the pitch, L_p . The measurement results are shown as red circles with error bars, and the dashed lines are obtained from the finite element simulations with different values of the sidewall thermal boundary resistance. The black solid line indicates the reference case when the samples have a layered structure as shown in the bottom right of the plot.

thickness of the nanostructured fin array layer, as measured by transmission electron microscopy. They also include the impact of aluminum oxidation on the interface between Al pillars and the top Al transducer and on the heat capacity of the Al transducer layer. (See Supplementary Information for uncertainty propagation and sensitivity analysis.)

The experimental results show that κ_{NFA} increases with decreasing pitch of the microfabricated pillars, as shown in Figure 2b. Specifically, κ_{NFA} for $L_P = 200$ nm is ~ 1.7 times that for $L_P = 1.6$ μm , more than two times the reference value with the same volume fraction of Al:SiO₂. This is mainly due to the increased contact area between Al and SiO₂ as the pitch L_P decreases. To understand the physical mechanisms responsible for this enhancement in effective conductance of the nanostructured fin array layer, we analyze the various thermal conduction channels through the sample stack. The heat injected into the Al transducer predominantly flows into the pillars due to the much smaller thermal resistance of the Al pillars compared to the surrounding SiO₂. The heat conducts three-dimensionally across the structured interface in the cross-plane (normal to the interface) and in-plane (parallel to the interface) directions. The in-plane heat flow contributes to the increase in the effective cross-plane thermal conductance of the nanostructured fin array layer as pitch L_P decreases.

Simulation of nanostructured fin array

We use finite element numerical simulations to further investigate thermal conduction in the nanostructured fin array. The effective thermal conductivity of the fin layer is calculated by solving the heat diffusion equation within a geometry shown in Figure 1 (see Supplementary Information for the details of the finite element simulations). To consider the size effects on the Al pillars, we treat Al pillars and the Al transducer layer to have separate thermal conductivity and the value for the pillars is obtained using a model based on the kinetic theory as discussed below. We use the same thermophysical properties for the other materials and interfaces as used in the TDTR model shown in Figure 2a.

Modeling thermal conductivity of nanostructured fin

We use a model based on the kinetic theory to estimate the reduction in the thermal conductivity of Al pillars with decreasing pitch. The thermal conductivity of Al is the summation of the electron and phonon thermal conductivities, and the bulk thermal conductivity of each carrier can be written as

$$\kappa_{\text{Al,bulk}} = \sum_s \int_0^\infty \frac{1}{3} C v \Lambda_{\text{bulk}} d\omega, \quad (1)$$

where C , v , and Λ_{bulk} are the volumetric heat capacity, velocity, and mean free path (MFP) of energy carrier in bulk Al, respectively. s is the band/mode index, and ω is angular frequency. As the pitch L_P decreases, there is an increase in boundary scattering of the energy carriers within the Al pillars; this effect becomes significant when the feature size approaches the MFP of bulk Al Λ_{Bulk} . The MFPs of the electrons range from 1 to 20 nm at 300 K, and the MFPs of the phonons span from ~ 1 to ~ 8 nm at 300 K [41]. The Al pillar thermal conductivity of each carrier is written as

$$\kappa_{\text{Pillar}} = \sum_s \int_0^\infty \frac{1}{3} C v \Lambda_{\text{Pillar}} d\omega. \quad (2)$$

By changing variables from ω to Λ_{bulk} , Eq. (2) becomes [42]

$$\kappa_{\text{Pillar}} = \int_0^\infty \left[- \sum_s \frac{1}{3} C_v \Lambda_{\text{bulk}} \left(\frac{d\Lambda_{\text{bulk}}}{d\omega} \right)^{-1} \right] \frac{\Lambda_{\text{Pillar}}}{\Lambda_{\text{bulk}}} d\Lambda_{\text{bulk}}, \quad (3)$$

where the term in square brackets is the contribution of each MFP to thermal conductivity. The MFPs of Al pillar Λ_{Pillar} are calculated using Matthiessen's rule, and the MFP is given by

$$\Lambda_{\text{Pillar}}^{-1} = d_{\text{grain}}^{-1} + \Lambda_{\text{bulk}}^{-1} + \Lambda_{\text{boundary}}^{-1}, \quad (4)$$

where d_{grain} is the averaged grain size, Λ_{bulk} is the MFP of bulk Al, and $\Lambda_{\text{boundary}}$ is the MFP caused by boundary scattering. We obtain the MFP distribution for bulk Al and its contribution to the thermal conductivity from Jain and McGaughey [41]. We use the measured Al transducer thermal conductivity to estimate the averaged grain size d_{grain} to be ~ 12 nm, which is within a typical range of grain sizes in an evaporated Al film [43, 44]. We note that the averaged grain boundary can be larger than the estimated grain size because the value includes the possible impact of impurity and imperfections. We assume that the grain size in the Al pillar is the same as in the transducer because the metallization conditions for the transducer and the pillars are identical. The MFPs due to boundary scattering, $\Lambda_{\text{boundary}}$, is calculated using a Monte Carlo approach [45, 46]. The thermal conductivity of Al pillars is estimated to be suppressed from ~ 92 to ~ 80 Wm $^{-1}$ K $^{-1}$ upon reducing the half pitch from 1 μm to 100 nm with 25% of the Al volume fraction, when the thickness of pillars is fixed to 65 nm. We note that the ballistic effect on Al pillars becomes significant when L_P is smaller than 200 nm. (See the Supporting Information for calculation details.)

Thermal conduction mechanisms in nanostructured interfaces

To identify the various thermal conduction pathways and determine how the resistance of each pathway changes with L_P , we conduct simulations for four different cases: sidewall thermal boundary resistances of 0, 5, 20 m ^{2} K GW $^{-1}$ and the limit of infinite thermal boundary resistance. In addition to thermal conduction normal to the plane, three different planar conduction pathways are involved, namely, constriction in the top Al, spreading in the SiO $_2$ fin array below, and conduction through sidewall interfaces within the nanostructured fin array as shown in Figure 3a. The contribution of each pathway to the net thermal conduction is a function of L_P . For instance, with decreasing L_P , the reduced travel distance for heat flux in the lateral direction leads to a decrease in the constriction and spreading resistances. The effect is an increase in κ_{NFA} with decreasing pitch for the case of infinite sidewall thermal resistance of sidewall interfaces as shown in Figure 2b.

The measured effective thermal conductivity of the nanostructured fin array layer is still higher than the computed κ_{NFA} value with infinite sidewall interfacial resistances. This difference is attributed to the impact of thermal conduction through sidewall interfaces. The effective conductivity κ_{NFA} depends on the thermal resistance of sidewall interfaces between the Al pillar and the SiO $_2$ in the fin layer, and the sensitivity increases with decreasing pitch. We note that thermal conduction through sidewall interfaces becomes a major conduction path, which rarely plays an important role in interfacial thermal conduction.

By comparing our experimental data with finite element simulations, we estimate that the thermal resistance of sidewall interfaces lies in the range 5 to 20 m ^{2} K GW $^{-1}$. This resistance of the sidewall interface is higher than the experimentally measured value of the Al-SiO $_2$ planar interface (4.4 m ^{2} K GW $^{-1}$) possibly due to anisotropic etching and directional metallization; however, the value is still within the typical range for many metal-dielectric interfaces [9, 47–49]. We note that these experimentally measured values are often larger than the theoretical predictions based purely on acoustic mismatch and phonon-electron coupling, mainly due to extrinsic factors such as near interfacial defects, roughness, and adsorbed impurities. As L_P decreases, thermal conduction through sidewall interfaces dominates the temperature distribution in the SiO $_2$ region of the nanostructured

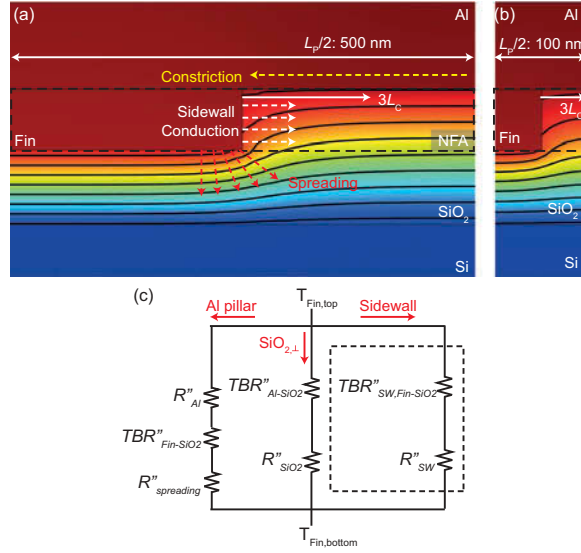


Figure 3. (a), (b) Temperature profiles corresponding to $L_p = 1 \mu\text{m}$ and $L_p = 200 \text{ nm}$, calculated using the finite element method. The black solid and dashed lines are isotherms and the boundary of the NFA, respectively. (a) The dashed arrows show the thermal conduction mechanisms within the stack. (c) Simplified thermal circuit model for the system showing the various thermal pathways including spreading resistance, across SiO₂ in the layer of nanostructured fin array, and sidewall interface. The subscripts Al and Fin indicate the transducer and metal embedded in SiO₂, respectively, and SW indicates sidewall. $T_{\text{Fin,top}}$ and $T_{\text{Fin,bottom}}$ are the averaged temperatures on the top and bottom boundaries of the fin layer.

fin array. Figure 3a shows the temperature distribution in the cross section of the unit cells for $L_p = 1 \mu\text{m}$ and $L_p = 200 \text{ nm}$. For $L_p = 200 \text{ nm}$, the lateral temperature gradient extends within the entire SiO₂ region between two adjacent fins, whereas for $L_p = 1 \mu\text{m}$ it is limited to the vicinity of the fin. This indicates that the embedding material of the nanostructured fin array layer, which is SiO₂ in this work, increasingly participates in cross-plane heat transfer as pitch decreases.

Thermal conduction through sidewall interfaces

Among the different thermal conduction pathways, transport across sidewall interfaces becomes a major conduction channel in the nanostructured interfaces as the pitch decreases. We estimate the thermal resistance offered to heat flow across the sidewalls of the Al pillars by analyzing the distribution of temperature and its gradient in their vicinity. This provides insights for relevant length scales of in-plane conduction, which can be useful in interface design. The mismatch in thermal conductivity between Al and SiO₂ works together with the local interface resistance and the geometry to induce lateral conduction. The contrasting thermal conductivities of the two materials, in this case Al and SiO₂ ($\kappa_{\text{Al}} = 94 \text{ W m}^{-1} \text{ K}^{-1}$ and $\kappa_{\text{SiO}_2} = 1.38 \text{ W m}^{-1} \text{ K}^{-1}$), sets up a temperature profile that exponentially decays in the in-plane direction with a characteristic length, L_c [33]. We build a simplified thermal circuit model for the nanostructured fin array based on the layered stack configuration in Figure 2b, and the circuit is shown in Figure 3c. We note that constriction resistance in the Al can be neglected compared to spreading resistance in the SiO₂ because the thermal conductivity of Al is ~ 70 times higher than that of SiO₂. Thermal resistance that is presented to heat flux going through sidewall interfaces is decoupled into the boundary resistance, TBR''_{SW} , and the resistance of SiO₂ in the pillar layer, denoted as R''_{SW} . The resistance R''_{SW} is approximately,

$$R''_{SW} \cong \frac{2L_C}{\kappa_{SiO_2}}. \quad (5)$$

The characteristic length L_C , known as the healing length along the layer of the nanostructured array, is $\sim \sqrt{t_{NFA} t_{SiO_2}/2}$, where t_{NFA} and t_{SiO_2} are the thicknesses of the fin array layer and contiguous SiO_2 layers, respectively [29, 33]. (See Supplementary Information for details of thermal circuit derivation and analysis.) For the geometries used in this work, $L_C \approx 50$ nm. We note that L_C should be smaller than $\sim L_P/12$ to have most of the temperature rise decay within the unit cell. When L_P is smaller than 600 nm, L_C is geometrically limited by the pitch and is therefore $\approx L_P/12$. In this regime, R''_{SW} becomes proportional to the pitch L_P , and the resistance with $L_P = 200$ nm is ~ 24 m² K GW⁻¹, which is comparable to TBR''_{SW} . With decreasing pitch, the boundary resistance TBR''_{SW} plays an increasingly important role in the conduction pathway across sidewall interfaces.

Design guidelines for nanostructured interfaces

We further explore the impact of the aspect ratio and pitch from the diffusive to quasiballistic transport regime in Al pillars, and this provides design guidelines for nanostructured interfaces. We calculate κ_{NFA} varying the aspect ratio t_{Pillar}/w_{Pillar} from 0.1 to 10 with $L_P = 40$ nm, 200 nm, and 1.0 μ m, where t_{Pillar} and w_{Pillar} are the thickness and the width of the Al pillars, respectively, as shown in the inset of Figure 4. The reduction in thermal conductivity of the Al pillars is calculated using a model based on the kinetic theory (see inset of Figure 4). The results of finite element calculations with pitch-dependent and constant Al thermal conductivity κ_{Pillar} are shown with solid and dashed lines, respectively. The impact of the aspect ratio can be grouped into two regimes: $t_{Pillar}/w_{Pillar} < 1$ and $t_{Pillar}/w_{Pillar} > 1$. When $t_{Pillar}/w_{Pillar} < 1$, κ_{NFA} increases very slowly with aspect ratio as shown in Figure 4, because the interfacial resistance of sidewall interfaces TBR''_{SW} is larger than the resistance of other conduction paths. On the other hand, when $t_{Pillar}/w_{Pillar} > 1$, κ_{NFA} increases rapidly with increasing aspect ratio, mainly due to the increased thermal conduction through sidewall interfaces. In this regime, the impact of the reduction in κ_{Pillar} becomes pronounced, as shown by the difference between solid and dashed lines in Figure 4. Even though

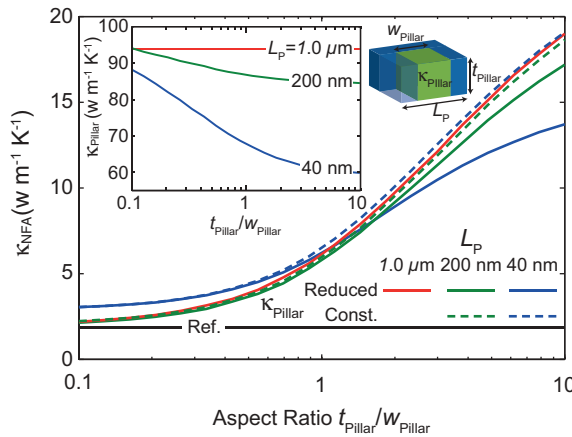


Figure 4. Effective thermal conductivity of the NFA κ_{NFA} with varying aspect ratios (defined as the ratio of the pillar thickness, t_{Pillar} , to the pillar width, w_{Pillar}). The Al: SiO_2 fill fraction in all cases is 25%, and TBR''_{SW} is set to 4.4 m² K GW⁻¹ for all interfaces between Al and SiO_2 . Solid and dashed lines denote κ_{NFA} calculated with pitch-dependent and constant Al thermal conductivity (κ_{Pillar}), respectively. The inset shows κ_{Pillar} as a function of aspect ratio ranging from 0.1 to 10. The red, green, and blue colors correspond to pitch $L_P = 1,000$ nm, 200 nm, and 40 nm, respectively. The black solid line indicates the reference layered structure as shown in Figure 2b.

the reduced thermal conductivity may negatively impact thermal conduction over the fin array, the enhancement due to increased contact area is beneficial for any aspect ratio. We note that κ_{NFA} collapses onto a single curve for the case of constant κ_{Pillar} when $t_{\text{Pillar}}/w_{\text{Pillar}} > 1$, though such convergence is not observed when $t_{\text{Pillar}}/w_{\text{Pillar}} < 1$ due to the nonnegligible spreading and constriction resistances. This analysis suggests that the concept of nanostructured interfaces can be extended to a combination of a diffusive medium and a quasiballistic medium despite a reduction in the thermal conductivity of the quasiballistic medium.

We note that if this idea must be extended to interfaces between two materials that both have long intrinsic mean free paths compared to the feature size, additional factors will need to be considered in the design process. Though nanostructuring the interface through fin-like projections will increase the thermal conductance, decreasing feature sizes could also lead to lower near-interfacial thermal conductivities in the adjacent materials. This suggests an optimum pitch where the total thermal conductance is maximized, when the competing effects of increased contact area and phonon size effects balance each other out. This merits further study and is the focus of ongoing work.

Concluding remarks

In the present work, we show that the solid-state nanostructured fin array is a new and promising approach to lower the thermal boundary resistance. We demonstrate that the nanostructured fin array with $L_p = 200$ nm enhances interfacial thermal conductance by more than a factor of two compared to an equivalent volume of stacked materials with a planar interface. The enhanced thermal conduction of the nanostructured fin array is immediately applicable to the design of near-junction layers for thermally limited electronics such as integrated nanoelectronics and silicon-on-insulator devices. Numerical simulations and theoretical calculations identify the contribution of the various conduction mechanisms in the nanostructured fin array, namely, constriction and spreading resistances and heat conduction across sidewalls. This highlights the role of sidewall interfaces in thermal transport for highly integrated nanosystems. We use a reduced-order analysis, which provides design guidelines for solid–solid interfaces. This simplified reduced-order model can also be applied to the complex simulation of many practical nanostructures, such as interconnects in microelectronics. We further discuss the impact of quasiballistic effects within the Al pillars in hypothetical, highly scaled fin arrays and show that the nanostructured fin array remains an effective solution in this regime.

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ORCID

Woosung Park  <http://orcid.org/0000-0001-9119-3781>

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