

Thermal Conduction across Metal–Dielectric Sidewall Interfaces

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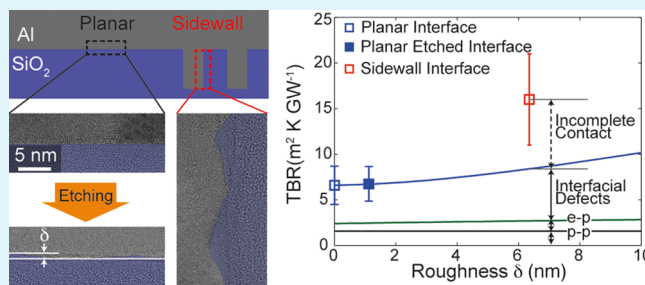
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S Supporting Information

ABSTRACT: The heat flow at the interfaces of complex nanostructures is three-dimensional in part due to the nonplanarity of interfaces. One example common in nanostructures is the situation when a significant fraction of the interfacial area is composed of sidewalls that are perpendicular to the principal plane, for example, in metallization structures for complementary metal-oxide semiconductor transistors. It is often observed that such sidewall interfaces contain significantly higher levels of microstructural disorder, which impedes energy carrier transport and leads to effective increases in interfacial resistance. The impact of these sidewall interfaces needs to be explored in greater depth for practical device engineering, and a related problem is that appropriate characterization techniques are not available. Here, we develop a novel electrothermal method and an intricate microfabricated structure to extract the thermal resistance of a sidewall interface between aluminum and silicon dioxide using suspended nanograting structures. The thermal resistance of the sidewall interface is measured to be $\sim 16 \pm 5 \text{ m}^2 \text{ K GW}^{-1}$, which is twice as large as the equivalent horizontal planar interface comprising the same materials in the experimental sample. The rough sidewall interfaces are observed using transmission electron micrographs, which may be more extensive than at interfaces in the substrate plan in the same nanostructure. A model based on a two-dimensional sinusoidal surface estimates the impact of the roughness on thermal resistance to be $\sim 2 \text{ m}^2 \text{ K GW}^{-1}$. The large disparity between the model predictions and the experiments is attributed to the incomplete contact at the Al–SiO₂ sidewall interfaces, inferred by observation of underetching of the silicon substrate below the sidewall opening. This study suggests that sidewall interfaces must be considered separately from planar interfaces in thermal analysis for nanostructured systems.

KEYWORDS: nonplanar interface, thermal boundary resistance, roughness, incomplete contact, electron–phonon coupling



1. INTRODUCTION

Interfaces dictate thermal transport in many nanostructured systems, such as fin field-effect transistors (FinFETs)^{1,2} and interconnects in microelectronics,^{3,4} and these interfaces are often found to be nonplanar. A nonplanar interface comprises two types of orthogonal surfaces: those that are parallel to the principal plane and sidewalls that are perpendicular to it. The quality of the sidewall interfaces can be lower than that of planar interfaces because of microstructural defects and has been shown to impact the electrical^{5,6} and the optical transport.^{7,8} However, despite the increasing prevalence of three-dimensional (3D) nanostructures having a large areal fraction of sidewalls, the quantitative differences between thermal transport across planar and sidewall interfaces have not been investigated.

Thermal interface resistance can originate from both “intrinsic” sources derived from dissimilar properties of the energy carriers between materials and “extrinsic” sources caused by the local microstructural quality of the interfaces. The theoretical lower bound of thermal interface resistance is dictated by the intrinsic sources, including the mismatch in the acoustic properties of the adjacent materials,⁹ and energy transfer between dissimilar energy carriers.^{9–12} The experimentally reported thermal interfacial resistance values are often larger than theoretical predictions primarily because of “extrinsic” sources consisting of interfacial defects (roughness),^{13–18} intermixing of atomic species,^{19,20} crystalline

Received: May 11, 2017

Accepted: August 8, 2017

Published: August 8, 2017

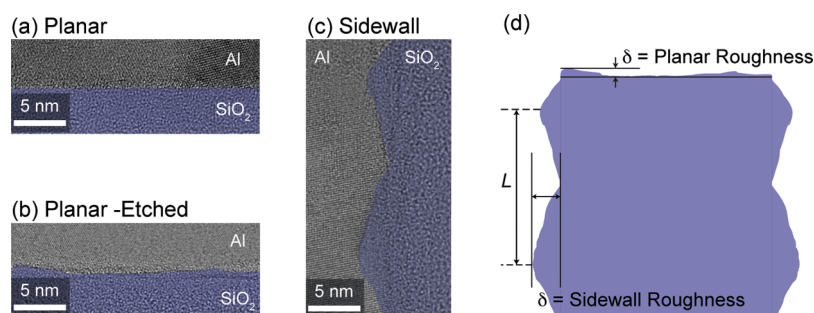


Figure 1. TEM images for (a) nonetched planar, (b) etched planar, and (c) sidewall interfaces between Al and SiO₂. The wavelength of roughness and the peak–peak roughness is defined as L and δ as shown in (d). The wavelength of the roughness is estimated as the distance between the adjacent peaks. We assume that $L = 15$ nm for both (b) and (c) and $\delta = \sim 1$ and ~ 6 nm for (b) and (c), respectively.

defects,^{21–23} and interfacial bonding strength.^{24–28} For sidewall interfaces in the present study, there is a significant contribution to the thermal interfacial resistance from extrinsic sources owing to the anisotropic fabrication processes, such as reactive ion etching (RIE) and directional material deposition that tend to degrade the quality of the microstructure at the sidewall.^{7,29}

While thermal transport across planar interfaces has been extensively studied,^{9,30–39} limited attention is given to the impact of sidewall interface. In this article, we develop a novel technique to characterize the thermal interface resistance of sidewall interfaces between metals and dielectrics, a common material combination in electronics such as interconnects. This provides a fundamental understanding on sources of interfacial resistance and quantification of the disparity in the thermal resistance of sidewall and planar interfaces.

2. THERMAL CHARACTERIZATION OF INTERFACES

We explore thermal transport across three types of interfaces between Al and SiO₂: planar, planar and etched, and sidewall interfaces as shown in Figure 1a–c, respectively. The planar interface provides a baseline value for interfacial resistances between Al and SiO₂, where Al is deposited on thermally grown SiO₂ using evaporation. The planar-etched interface is treated with RIE process followed by the same metal deposition. Sidewall interfaces are fabricated using the identical etching and metallization processes as those for the planar-etched interfaces. The etching process degrades the quality of the interface, specifically for sidewall interfaces, and the roughened interfaces are observed using transmission electron microscopy (TEM) as shown in Figure 1 (see the Supporting Information for sample fabrication). We characterize the planar and etched planar interfaces using the time-domain thermoreflectance (TDTR) technique.^{21,40,41} Conducting measurements on sidewall interfaces is significantly more challenging and requires elaborate microfabricated structures.

Here, we develop an electrothermal method and an intricate microfabricated structure containing a high density of sidewall interfaces along the conduction path to extract the thermal resistance of a sidewall interface between Al and SiO₂. We design and fabricate the suspended nanograting structures of alternating Al and SiO₂ for the electrothermal characterization of sidewall interfaces as shown in Figure 2. Four of the Al lines are selectively patterned into the four-probe measurement configurations to serve as either a Joule heater or local thermometers, and these lines are connected to contact pads to provide electrical access. The length of the grating structures perpendicular to the metal lines is 10 times more longer than in

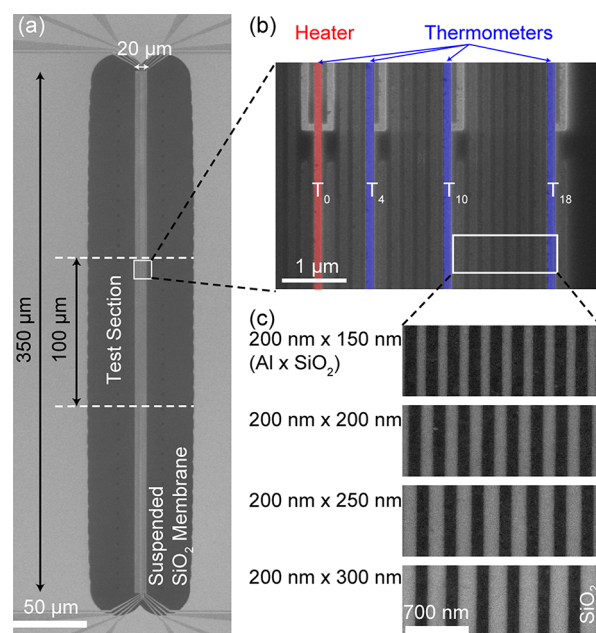


Figure 2. Sample geometry for the thermal resistance of a sidewall interface measurement structure. (a) Scanning electron microscopy (SEM) image depicting the entire suspended region of structure. The dark region indicates the suspended region, and the measurement region is between dashed lines. (b) Higher magnification SEM image shows the location of the heater (false color red line) in the center of the grating structure, and the grating structure is symmetric with respect to the heater line. Thermometers (false color blue lines + red line) are located at 0, 4, 10, and 18 unit cells and referred to as T_0 , T_4 , T_{10} , and T_{18} , respectively. (c) SEM images for various combinations of the material width, and the images are taken prior to device suspension.

the parallel direction. The high aspect ratio of the grating structures and suspended film confines heat to travel laterally through suspended alternating lines of Al and SiO₂ and therefore through each of the sidewall interfaces.⁴² The symmetry of the grating structures with respect to the central heater line ensures that half of the heat flows outward in each direction. The width of the SiO₂ layers varied between 150 and 300 nm enables us to subtract out the volumetric contribution of the SiO₂ layers, which is similar to the transmission line measurement for electrical contact resistance.⁴³ The range of SiO₂ layer widths is designed to set the volumetric thermal resistance of each SiO₂ layer to be comparable to the thermal resistance of a sidewall interface.

For thermal characterization, a dc electrical current is applied to generate Joule heating on the central heater line, and the temperatures at four different locations are measured using the heater and the thermometers. These thermometers are located at $n = 0, 4, 10$, and 18 , where n is the integer number of unit cells (i.e., an Al and SiO₂ bilayer) separating the thermometer n and the heater. The locations are shown in Figure 2b. With increasing power, the temperature differences between the heater and thermometers are measured. The temperature difference between the heater and the thermometer n is given by $\Delta T_{0-n} = T(0) - T(n)$, and for the constant thermal resistance of the nanograting structure, ΔT_{0-n} linearly increases with applied heating power. The temperature differences between the heater and the individual thermometers linearly increase with increasing heat input, as shown in Figure 3a. We obtain the thermal resistance for the different number of unit cells from the power–temperature slope and further extract the value for a single unit cell. The thermal resistance between the heater and the thermometer n , $R_{th,0-n}''$, is

$$R_{th,0-n}'' = \frac{dR_{e,0}}{dq''} \cdot \frac{dT_0}{dR_{e,0}} - \frac{dR_{e,n}}{dq''} \cdot \frac{dT_n}{dR_{e,n}} \quad (1)$$

where the subscripts e and th denote electrical and thermal resistances, respectively, and $dT_0/dR_{e,0}$ and $dT_n/dR_{e,n}$ are obtained from separate temperature-dependent electrical resistance measurements between 295 and 320 K. We then extract the thermal resistance per unit cell $R_{th,unit}''$ by measuring the slope of the linear function $R_{th,0-n}''$ versus the number of unit cells n .

The thermal resistance of a single unit cell comprises three components, which include the volumetric thermal resistances of the SiO₂ layer R_{th,SiO_2}'' , the Al layer $R_{th,Al}''$, and the thermal resistances at both sidewall interfaces $R_{Int,SW}''$

$$R_{th,unit,total}'' = R_{th,Al}'' + R_{th,SiO_2}'' + 2 \cdot R_{Int,SW}'' \quad (2)$$

The contribution of the Al and SiO₂ layers needs to be separated out to extract the thermal boundary resistance (TBR) of sidewall interfaces. We estimate the thermal conductivity of the Al layer to be $\sim 120 \text{ W m}^{-1} \text{ K}^{-1}$ from the measured electrical resistivity using the Wiedemann–Franz law with the universal Lorentz number of $2.44 \times 10^{-8} \text{ W } \Omega \text{ K}^{-2}$. The contribution from the Al layer (note that $R_{th,Al}''$ is less than $\sim 1\%$ of $R_{th,unit}''$) is then subtracted from the total thermal resistance. This simplifies eq 2 to contain only the volumetric thermal resistance of the SiO₂ layer and the two thermal resistances from the sidewall interfaces

$$R_{th,unit}'' = \left(\frac{1}{k_{SiO_2}} \right) \cdot w_{SiO_2} + 2 \cdot R_{Int,SW}'' \quad (3)$$

We obtain $R_{th,unit}''$ with four different width combinations between Al and SiO₂ as shown in Figure 2c. The thermal resistance of the sidewall interface is extracted by extrapolating the resistance of a unit cell with the width of SiO₂, w_{SiO_2} , as shown in Figure 3b. The y-intercept of the linear fit equals twice the sidewall TBR. The sidewall thermal interface resistance between the Al and thermal SiO₂ layers is found to be $\sim 16 \pm 5 \text{ m}^2 \text{ K GW}^{-1}$. The slope of eq 2 yields the inverse of the thermal conductivity of SiO₂, and we extract a value of $k_{SiO_2} = \sim 1.4 \pm 0.1 \text{ W m}^{-1} \text{ K}^{-1}$, which agrees with the literature value for thermally grown SiO₂ to within $\sim 1\%$.^{44–46} This confirms the accuracy of the electrothermal measurements of this work. The thermal conductivity of the SiO₂ layer is independent of the layer width because the spatial dimensions in this measurement are much greater than the SiO₂ phonon mean free paths (MFPs).^{44,47} The uncertainty in $R_{th,SW}''$ is predominantly due to the uncertainty in w_{SiO_2} , which comes from the interfacial roughness and TEM resolution limit. The uncertainty in w_{SiO_2} is calculated to be $\sim 13 \text{ nm}$, and this uncertainty in w_{SiO_2} propagates to $\sim 4.4 \text{ m}^2 \text{ K GW}^{-1}$ of uncertainty in $R_{th,SW}''$. Other sources of uncertainty, such as parasitic heat loss along the grating structure and radiation, contribute less than 6% error to the measurement (see the Supporting Information).

Two planar interface samples are prepared using the same oxide growth and Al deposition conditions as the nanograting structure for thermal resistance measurements of sidewall interfaces. One planar interface is treated by etching SiO₂ before Al deposition with the same etching conditions as the nanograting structure for sidewall thermal interface resistance

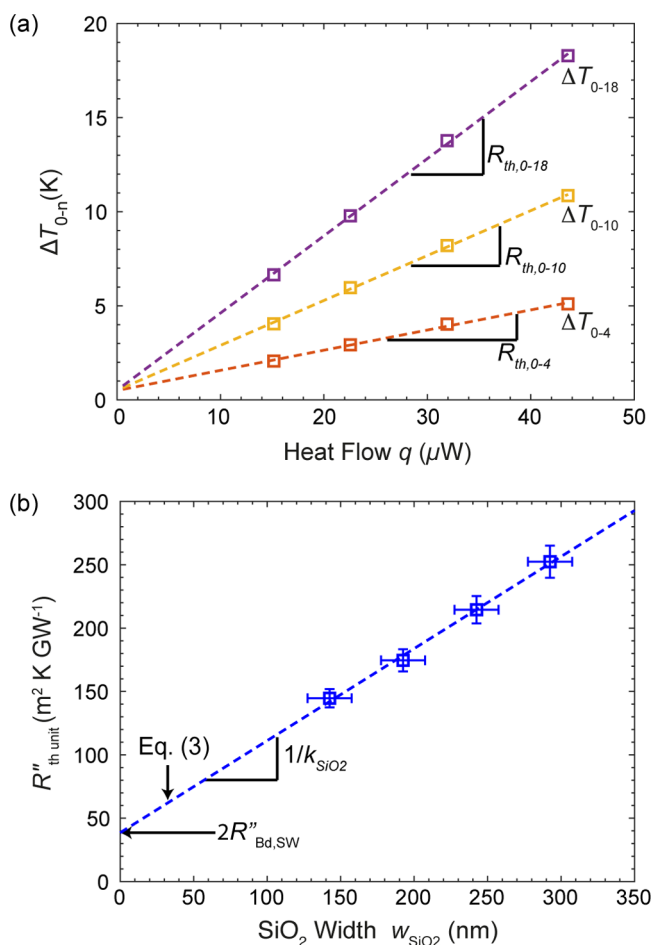


Figure 3. (a) Experimentally measured temperature difference between the heater and the thermometers, denoted as ΔT_{0-n} , where n is the number of unit cells separating the thermometer from the heater. (b) Measured thermal resistances of the unit cells with various widths of SiO₂, where the contribution of Al has been removed. The dashed line is a linear fit to the data points. The slope of the trend line is the inverse thermal conductivity of SiO₂, k_{SiO_2} , and the y-intercept indicates the total TBR contribution from both sidewalls between Al and SiO₂.

measurements, whereas the other has no treatment on the interface. This is followed by depositing ~ 91 nm thick Al using electron-beam evaporation on top of the thermally grown SiO_2 (without etching process). The planar interface between Al and SiO_2 is investigated using TDTR, an optical pump–probe technique for measuring the thermal interface resistance in multilayer thin-film structures.^{21,40} We find the thermal interface resistance across the planar Al– SiO_2 interface to be $\sim 6.6 \pm 2.2 \text{ m}^2 \text{ K GW}^{-1}$ for the unetched region and $\sim 6.7 \pm 1.9 \text{ m}^2 \text{ K GW}^{-1}$ for the etched region. Uncertainties in the extracted values are propagated from the uncertainties in the Al transducer layer thickness and the thermal properties of the Al and SiO_2 layers (see the Supporting Information).

3. RESULTS AND DISCUSSION

The measured planar thermal interface resistance values are only $\sim 40\%$ of the thermal resistance of the sidewall interface. We attribute this discrepancy primarily to extrinsic factors, increased roughness, and incomplete contacts at sidewall interfaces. A comparison between the planar (Figure 1a) and the planar-etched (Figure 1b) interfaces shows that the etching process increases the interface roughness, and the roughness become more pronounced on the sidewall interfaces, as shown in Figure 1c. While the planar interfaces of both the etched and nonetched samples have perfect interfaces and ~ 1 nm peak–peak roughness, respectively, the sidewall interfaces exhibit ~ 6 nm peak–peak roughness as measured using TEM images shown in Figure 1.

This increased roughness impacts the transport properties of energy carriers and defects in the interfacial region. In addition to the roughness, the quality of the contact between Al and SiO_2 at the sidewall interfaces is imperfect as evidenced by the undercut silicon below the sidewall interfaces, indicating that pathways exist at the sidewall interfaces that allow etchants to pass through (see the Supporting Information). The incomplete contact at the sidewall interfaces constitutes an additional source of sidewall thermal interface resistance.

To understand the impact of roughness and the incomplete contact, we deconstruct the thermal interface resistance depending on its source as follows

$$R''_{\text{total}} = R''_{\text{Int,p-p}} + R''_{\text{Int,e-p}}(\delta) + R''_{\text{Ext,defects}}(\delta) + R''_{\text{Ext,contact}} \quad (4)$$

where the argument δ is the peak–peak roughness, the subscript p–p indicates phonon–phonon energy transfer across an interface, e–p indicates electron–phonon coupling resistance in Al, *defects* indicates the interfacial structural defects, and *contact* indicates incomplete contact. The components $R''_{\text{Int,p-p}}$ and $R''_{\text{Int,e-p}}$ are intrinsic sources of thermal interface resistance corresponding to imperfect energy transfer between dissimilar materials. The remaining terms correspond to extrinsic resistance factors because of the interfacial microstructure.

We individually estimate the components in thermal resistances from both intrinsic and extrinsic sources as shown in Figure 4, which provides a quantitative comparison between the planar and the sidewall thermal interface resistances. We use the diffuse mismatch model to assess the phonon–phonon resistance $R''_{\text{Int,p-p}}$ giving a value of $\sim 1.6 \text{ m}^2 \text{ K GW}^{-1}$ for the Al– SiO_2 interface, which is ~ 25 and $\sim 10\%$ of the thermal resistance for the planar and sidewall interfaces, respectively. In this model, we assume that SiO_2 has the same acoustic characteristics as quartz due to their similar atomic composition

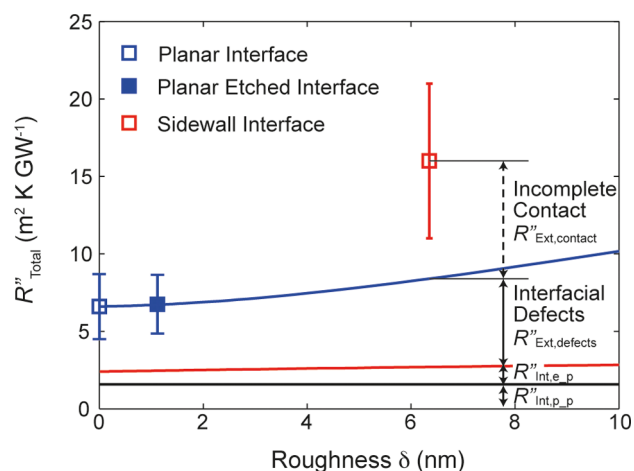


Figure 4. Thermal interface resistance values for both sidewall and planar interfaces of Al/ SiO_2 , where δ is peak–peak roughness. The solid lines are obtained from model predictions, and the dashed arrow indicates the contribution of incomplete contact to the thermal resistance of sidewall interfaces.

and also use the Debye approximation (see the Supporting Information).

To estimate the contribution of electron–phonon coupling and near interfacial defects to thermal interface resistance, we first model the rough surface as having a two-dimensional

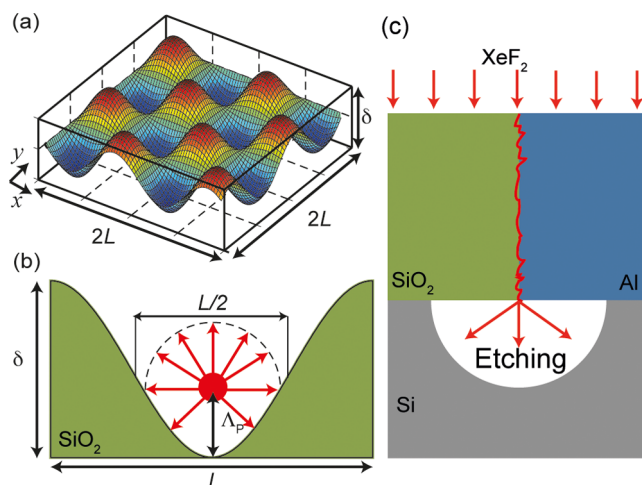


Figure 5. (a) A roughness model in 3D, showing 2×2 unit cells, where L is the wavelength of a unit cell, and δ is peak–peak roughness. (b) Schematic showing increased phonon boundary scattering in the valley between rough structures. The red filled circle represents phonons at a distance of a phonon MFP Λ_p from the surface. $L/2$ is the mean lateral characteristic length scale induced by rough geometry. (c) Schematic of incomplete contact of sidewall interfaces, which becomes a pathway for XeF_2 gas to reach the underlying Si.

sinusoidal profile as shown in Figure 5a. The local height f with respect to the interfacial plane is given by

$$f(x, y) = \frac{\delta}{2} \sin\left(\frac{2\pi}{L}x\right) \sin\left(\frac{2\pi}{L}y\right) \quad (5)$$

where L is the wavelength in both x and y directions and δ is the peak–peak amplitude of roughness. We use TEM to estimate L and δ as shown in Figure 1. L is ~ 15 nm for both

the etched planar and sidewall interfaces, and δ is ~ 1 and ~ 6 nm for the etched planar and the sidewall interfaces, respectively.

We evaluate the thermal resistance of electron–phonon coupling in Al $R''_{\text{Int,e-p}}$ with rough interfaces because the dominant thermal energy carriers are dissimilar between Al and SiO₂. We begin by estimating the lattice thermal conductivity of Al, which is a key parameter in $R''_{\text{Int,e-p}}$. The lattice thermal conductivity of pure Al (i.e., only phonon–phonon and electron–phonon scattering exist) $k_{\text{p,Al}}$ is reported to be 6 W m^{−1} K^{−1} based on ab initio calculations.⁴⁸ However, the lattice thermal conductivity in this work is smaller than that of the ideal material as phonons experience additional scattering with grains and rough structure of the interface. The average grain size of Al is estimated to be ~ 40 nm by comparing the electron thermal conductivities from both first-principle calculations and experiments using the Wiedemann–Franz law. We also quantify average grain size using TEM images, and the value agrees well with the estimated value from electrical measurements. The grain size is in the typical range of Al layer that is deposited using electron-beam evaporation^{49,50} (see the Supporting Information for grain size quantification). Al phonons are subjected to scattering with rough structures as shown in Figure 5b, and the half wavelength of roughness $L/2$ provides the length scale of the increased scattering in the roughness valley. The resulting phonon MFP of Al in the interfacial region becomes

$$\lambda_{\text{p,Al, reduced}}^{-1} = \lambda_{\text{p,Al}}^{-1} + D_{\text{grain}}^{-1} + (L/2)^{-1} \quad (6)$$

where $\lambda_{\text{p,Al}}$ is the average phonon MFP in Al ($\lambda_{\text{p,Al}} \approx 4$ nm).⁴⁸ With additional scattering, the lattice thermal conductivity is suppressed from 6 to ~ 3.6 W m^{−1} K^{−1}. The thermal interface resistance due to electron–phonon coupling, $\text{TBR}_{\text{Int,e-p}}$, is estimated to be $(G_{\text{Al}} k_{\text{p,Al, reduced}})^{-1/2}$,¹⁰ where G_{Al} is the electron cooling rate in Al and is obtained from the literature to be 24.5×10^{16} W m^{−3} K^{−1}.¹¹ The thermal resistance due to electron–phonon coupling in Al becomes ~ 1.1 m² K GW^{−1} for the sidewall interface.

The combination of $R''_{\text{Int,p-p}}$ and $R''_{\text{Int,e-p}}$ is the theoretical limit of thermal interface resistance for Al–SiO₂ interfaces, which is $\sim 40\%$ of the experimentally measured planar thermal interface resistance. We attribute this difference to the extrinsic sources of thermal interface resistance such as impurities or near interfacial defects because thin-film metals deposited by evaporation contain a high density of defects.^{21,51} It has been reported that experimentally measured thermal interface resistances increase with interfacial roughness.^{15,52,53} To explain the impact of roughness, we assume that the areal density of imperfections is locally constant and that $R''_{\text{Ext, defects}}$ is proportional to the total contact area of interfaces. The thermal interface resistance due to defects is given by

$$R''_{\text{Ext, defects}} = \gamma \sigma_0 \varepsilon_{2D} \quad (7)$$

where γ is the coefficient that relates the density of defects to thermal interface resistance, σ_0 is the areal defect density for smooth interfaces, and ε_{2D} is the contact area ratio between the rough and smooth interfaces. We calculate $\gamma \sigma_0$ from the difference between the measured thermal interface resistance of the nonetched planar sample and theoretical prediction due to just the intrinsic sources. The contact area ratio per unit cell for the sinusoidal roughness is calculated using eq 4, and the ratio is given by

$$\varepsilon_{2D} = \frac{1}{L^2} \iint_{x=0, y=0}^{x=L, y=L} \sqrt{\left(\frac{\partial f}{\partial x}\right)^2 + \left(\frac{\partial f}{\partial y}\right)^2 + 1} \, dx dy \quad (8)$$

For $L = 15$ nm and $\delta = 6$ nm, $\varepsilon_{2D} \cong 1.35$, meaning that the contact area is increased by 35% relative to the planar interface, and the contribution of interfacial defects to the sidewall thermal interface resistance increases accordingly.

We find that the combination of thermal interface resistance from intrinsic sources and that from interfacial defects underpredicts the thermal resistance of the sidewall interface as shown in Figure 4. This degraded interface quality is attributed to the incomplete contact at sidewall interfaces. The presence of this incomplete contact is inferred by our observation of undercut regions in Si below Al–SiO₂ sidewall interfaces, as indicated in Figure 5c. XeF₂, the etchant used to remove Si beneath the nanograting structures, minimally reacts with both Al and SiO₂,⁵⁴ implying that any access to the underlying Si must be through sidewall interfaces. This incomplete contact is mainly due to directional metal deposition using the electron-beam evaporation process, in contrast to more conformal processes such as atomic layer deposition. The difference between the measured thermal resistance of the sidewall interface and the prediction using the roughness model is attributed to the incomplete contact, and the impact of this incomplete contact on the thermal resistance of sidewall interfaces is assessed to be $\sim 48\%$, which is the largest contribution to the thermal interface resistance.

4. CONCLUSIONS

In summary, we develop a method to directly characterize the thermal resistance of sidewall interfaces between dielectrics and metals that are commonly found in FinFETs, interconnects, and other modern electronic devices. Using nanofabricated suspended grating structures, we measure the thermal resistance of the sidewall interface between Al and SiO₂ and find the value to be ~ 16 m² K GW^{−1}. This thermal resistance of the sidewall interface is observed to be ~ 2.5 times larger than that of the equivalent planar Al–SiO₂ interfaces. The discrepancy is attributed to roughness and incomplete contact at the sidewall interfaces. The roughness at the sidewall interface is generated by the RIE process required to fabricate such a structure, and the directional metallization process leads to the incomplete sidewall contact. These anisotropic processes are commonly used to increase the aspect ratio of devices in electronics, photonics, and microelectromechanical systems.^{55–57} This work suggests that further attention to sidewall roughness and interfacial quality is required to properly analyze thermal transport in modern electronics.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b06567.

Additional information on fabrication and experimental details of measurement devices for sidewall interfaces, experimental details of TDTR for planar interfaces, uncertainty analysis, diffuse mismatch model, quantification of averaged grain size, and evidence for incomplete contact of sidewall interfaces (PDF)

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors acknowledge the financial support from the Semiconductor Research Corporation (Agreement no. 2012-OJ-2308 titled: Thermal Properties of Nonplanar and Nanopatterned Interfaces for CMOS Beyond the 11 nm Node) and the government support under and awarded by the United States Department of Defense, Air Force Office of Scientific Research, National Defense Science and Engineering Graduate (NDSEG) Fellowship, 32 CFR 168a. Part of this work was performed at the Stanford Nano Shared Facilities (SNSF), supported by the National Science Foundation under award ECCS-1542152. The authors acknowledge the use of the SNSF of Stanford University for sample preparation and characterization.

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